2004 Paper 9 Question 2

VLSI Design

(*a*) Sketch designs for an n-input NAND gate in CMOS using

(*i*) static CMOS;

(*ii*) dynamic CMOS;

(*iii*) pseudo-nMOS. [2 marks each]

(*b*) Assuming that a conducting p-channel has a resistance γ times that of a similarly sized n-channel, annotate each of your circuit diagrams with suitable widths for the transistors, and explain the reasons for their values. [2 marks each]

(*c*) For each design, calculate the logical effort and the parasitic delay. [2 marks each]

(*d*) Which is likely to be fastest for the case when $n = 4$ and $\gamma = 3$? What difference would it make if the circuit were driving a large capacitative load? [2 marks]