2004 Paper 7 Question 7

Specification and Verification II

(a) Explain how combinational and sequential devices can be modelled in higher order logic in a uniform way (i.e. so that combinational and sequential devices can be connected).   [3 marks]

(b) Illustrate your explanation by showing how to define combinational devices NOT and AND that perform negation and conjunction, respectively, and a sequential unit-delay device DEL such that the output of DEL at time $t+1$ is the value input at t.   [3 marks]

(c) Define in higher order logic a predicate Rose such that if $t > 0$ then Rose f t is true if and only if f has a rising edge at time t (i.e. f is true at t but false at $t-1$).   [2 marks]

(d) Draw a diagram showing how to connect instances of NOT, AND and DEL to implement a device RoseImp, with one input and one output, such that the output is true at time t, where $t > 0$, if and only if there is a rising edge on the input at time t.   [6 marks]

(e) Represent your diagram in higher order logic by defining a predicate RoseImp, and then outline how to show that:

$$\forall in\ out.\ \mathsf{RoseImp}(in, out)\ \Rightarrow\ \forall t.\ out(t+1) = \mathsf{Rose}\ in\ (t+1)$$

You need not give a detailed proof, just an overview of how such a proof could be performed.   [6 marks]