2003 Paper 9 Question 2

VLSI Design

Explain the operation of ripple carry and carry-skip in a binary adder.   [4 marks]

Assuming a delay of τ for each stage of combinational logic (consisting of negation, product and sum), estimate the delays involved in calculating the most significant bit of the sum and the final carry-out of an n-bit adder using

(*a*) ripple carry

(*b*) carry-skip arranged in b blocks of k bits.   [4 marks]

What block size minimises the overall delay for a carry-skip adder?   [2 marks]

Explain how a variable block size can reduce the overall delay. Compare the delays for a 64-bit adder using fixed and variable block sizes.   [4 marks]

An alternative approach is to build a hierarchy of skip units in the style of a carry-lookahead tree. Derive equations for the skip units and estimate the delay in a 64-bit adder arranged as two 4-bit blocks, three groups of four 4-bit blocks (where each group has a higher level skip), and a further two 4-bit blocks.   [6 marks]