2003 Paper 8 Question 1

Comparative Architectures

The data sheet for a new workstation CPU tells you simply that it has a 8KB L1 data cache and 512KB L2 cache. As an inquisitive computer scientist, you wish to learn more about the system's memory hierarchy.

(*a*) Devise a method for determining the cache line size. You may assume that the L1 and L2 caches use the same line size, and that the operating system provides a microsecond accurate time function. Provide high-level language pseudo code of any test programs you would use, and describe how you would interpret their output. [6 marks]

(*b*) Describe how you produce an accurate estimate for the load latency incurred by accesses to the two caches and main memory. [6 marks]

(*c*) Outline a method you could use to determine the associativity of the caches. [8 marks]