2003 Paper 2 Question 3

Digital Electronics

(*a*) Design a 2-bit multiplier for unsigned integers which takes input $x_1\,x_0$ representing the unsigned integer X, $y_1\,y_0$ representing the unsigned integer Y, and produces the output $z_3\,z_2\,z_1\,z_0$ representing the unsigned integer Z. [4 marks]

(*b*) How can multipliers designed in part (*a*) be cascaded (with adders) to provide a four-bit multiplier? [4 marks]

(*c*) Design a sequential 8-bit multiplier. You can assume that a 16-bit adder has been provided. The finite state control can be described by a state diagram. [8 marks]

(*d*) Outline the design of a sequential divider which can divide 16-bit unsigned integers by 8-bit unsigned integers. [4 marks]