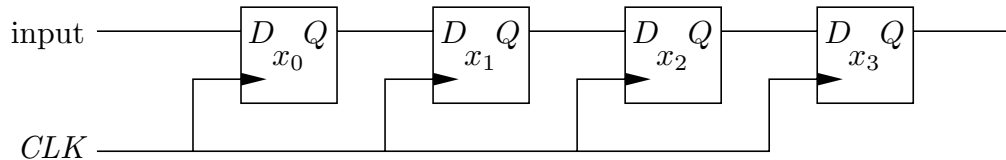


2003 Paper 2 Question 2

Digital Electronics

- (a) A 4-bit shift register constructed from edge-triggered D-type flip flops is shown below. If, on successive rising edges of the clock signal CLK , the input takes on the values 1, 0, 1, 0, 1, 1, 1, 0, what are the contents of the shift register after each edge of the clock? You may assume that the register contains all zeroes initially.



[4 marks]

- (b) Using a (possibly larger) shift register, show how one may detect a particular pattern in the input shown. As an example, use the 8-bit pattern 0xF0. High-order bits precede low-order bits in the input stream. [4 marks]
- (c) The input stream is framed by a one byte frame pattern (0xF0) every 256 bytes. However, the frame pattern may also appear at an arbitrary position in the input stream.

It is required to design a framing circuit which generates two outputs: *framelock*, which is asserted when the circuit “believes” it has determined where the frame boundaries are, and *frame pointer*, which is asserted on the clock edge immediately after the frame marker is detected. The circuit “believes” itself to be locked to the frame structure when two successive frame patterns have been found 256 bytes (i.e. 2048 bits) apart. The circuit should not respond to unaligned frame patterns while it believes itself to be in lock or if, once in lock, it has missed fewer than two expected frame patterns.

Draw a state diagram for the finite state control of the circuit. You may assume the existence of an 11-bit resettable counter. You should consider the process of assuming lock, maintaining lock and the accommodation of a single missed framing pattern. State explicitly any additional assumptions you make.

[10 marks]

- (d) Outline the complexity in gates and flip flops for an implementation of the framing circuit. [2 marks]