2002 Paper 5 Question 2

Computer Design

Modern dynamic random access memories (e.g. DRAM, SDRAM and RAMBUS) all support burst mode read and write access.

(a) Give an outline of the bus activity for a burst mode read access. [4 marks]

(b) Explain the difference between a direct mapped cache and an associative cache. [4 marks]

(c) What cache line replacement policies are typically used for a direct mapped cache and a set associative cache? [4 marks]

(d) Why are caches able to exploit burst mode accesses, and why is a write buffer often used? [4 marks]

(e) What is *bus snooping* and what does it achieve? [4 marks]