2002 Paper 4 Question 3

ECAD

A naïve Verilog programmer has written the following code in an attempt to implement an up–down counter. The correct behaviour should be:

- The counter should increment once each time the `up` button is pressed.
- The counter should decrement once each time the `down` button is pressed.
- The `error` flag should be set if both buttons are pressed at the same time.
- The `error` flag and `counter` should be set to zero when `reset` is high.
- The counter should be 8 bits in length.
- The input buttons are asynchronous and supply "1" when pressed, "0" when not pressed.

```
module UpDownCounter(clk, reset, up, down, count, error)
  input  clk;      // input clock
  input  reset;    // reset
  input  up;       // from the up button
  input  down;     // from the down button
  output counter;  // output the count value
  output error;    // error flag (1=error, 0=no error)

  reg [7:0] counter;
  always @(posedge clk) {
    if(reset) {
      counter <= 0;
      error   <= 0;
    }
    if(up)   counter <= counter + 1;
    if(down) counter <= counter - 1;
    if(up && down) error <= 1;
  }
endmodule
```

(*a*) Explain what is wrong with the above Verilog code. [10 marks]

(*b*) Write a corrected and commented version of the `UpDownCounter` module including any ancillary modules. [10 marks]