

## 2001 Paper 7 Question 2

### Specification and Verification II

- (a) Describe the difference between the simple and threshold switching models of transistors. [4 marks]
- (b) Give and explain an example of a circuit that illustrates when the threshold switching model is superior to the simple switching model. [4 marks]
- (c) Describe how combinational devices can be modelled as zero-delay sequential devices. When is this appropriate? [4 marks]
- (d) Write down a CTL formula expressing the property: *Ack is true on all paths sometime between 2 units and 5 units of time later.* [4 marks]
- (e) Describe how an edge-triggered D-type register can be abstracted to a unit delay. Give the formula in higher-order logic that expresses the abstraction. [4 marks]