2000 Paper 7 Question 9

Specification and Verification II

Define a predicate Rise such that Rise $clk\ t$ is true if and only if there is a rising edge on clk at time t. [2 marks]

Consider the following definition of the behaviour of a register in higher order logic:

$$\text{DFF}(q, d, clk, ce, ar, spare) =$$
$$(q\ 0 \ = \ \text{F}) \wedge$$
$$\forall t.$$
$$(\texttt{if Rise}\ clk\ t\ \vee\ \text{Rise}\ ar\ t$$
$$\texttt{then (if}\ ar(t{+}1)$$
$$\texttt{then}\ q(t{+}1)\ =\ \text{F}$$
$$\texttt{else (if}\ ce(t{+}1)\ \texttt{then}\ q(t{+}1)\ =\ d\ t\ \texttt{else}\ q(t{+}1) = q\ t))$$
$$\texttt{else}\ q(t{+}1) = q\ t)$$

Describe in detail the behaviour of $\text{DFF}(q, d, clk, ce, ar, spare)$. [6 marks]

Describe how circuit structures can be represented in logic. Explain how internal lines are modelled. [6 marks]

Consider a device $\text{D}(q, d, clk)$ with inputs clk and d and output q that is implemented using a DFF by connecting the ce line to power and the ar line to ground. Draw a diagram of this circuit and write down the corresponding logical formula. Derive a simplified formula for $\text{D}(q, d, clk)$. [6 marks]