# 2000 Paper 4 Question 5

## ECAD

A naïve Verilog programmer has made two attempts at implementing a `RandomBits` module. The module is supposed to generate a pseudo-random sequence of bits.

```
module RandomBitsA( rand_bits );
  output rand_bits;
  wire   [3:0] shift_reg;
  wire   newbit = ~(shift_reg[3] ^ shift_reg[1] ^ shift_reg[0]);
  assign shift_reg[3] = shift_reg[2];
  assign shift_reg[2] = shift_reg[1];
  assign shift_reg[1] = shift_reg[0];
  assign shift_reg[0] = newbit;
  assign rand_bits = newbit;
endmodule

module RandomBitsB( clk, rand_bits );
  input  clk;
  output rand_bits;
  reg    [3:0] shift_reg;
  wire   newbit = ~(shift_reg[3] ^ shift_reg[1] ^ shift_reg[0]);
  always @(posedge clk) begin
    shift_reg[3] <= shift_reg[2];
    shift_reg[2] <= shift_reg[1];
    shift_reg[1] <= shift_reg[0];
    shift_reg[0] <= newbit;
  end
  assign  rand_bits = newbit;
endmodule

// TestRandom is the top level module
module TestRandom( clk, tstA, tstB );
  input  clk;                   // input clock
  output tstA, tstB;            // output test bits
  RandomBitsA randa( tstA );
  RandomBitsB randb( clk, tstB );
endmodule
```

(*a*) In Verilog, what is the difference between continuous assignment and non-blocking assignment? [4 marks]

(*b*) What are the circuit diagrams corresponding to `RandomBitsA` and `RandomBitsB`? [8 marks]

(*c*) What is the output from `RandomBitsA` and `RandomBitsB`? [8 marks]