

Morello SoC (WIP)

- SODIMM DDR4 3200 x2 (72pin)
- 51.2 GBytes/s
- Modifications to ECC to store capability bit

- Mid-range GPU
- Single shader
- 256KByte L2

- Quad Arm core with capabilities
- L1/L2 cache modifications to proliferate capability bit

- Thin Links to FPGA
- Facilitates a broader set of IO not contained within the SoC itself

- High-end PCIe configuration
- x16 PCIe CCIX enabled
- x16 PCIe IO
- Can't carry capability tags

- Display processor
- Single display output
- Digital 8:8:8 RGB Output
- UXGA60 : 1600 x 1200

- SCP & MCP System control including boot

