Single Chip for 480RGBx272 TFT Panel 720x544 Driver with Timing Controller

Preliminary Specification

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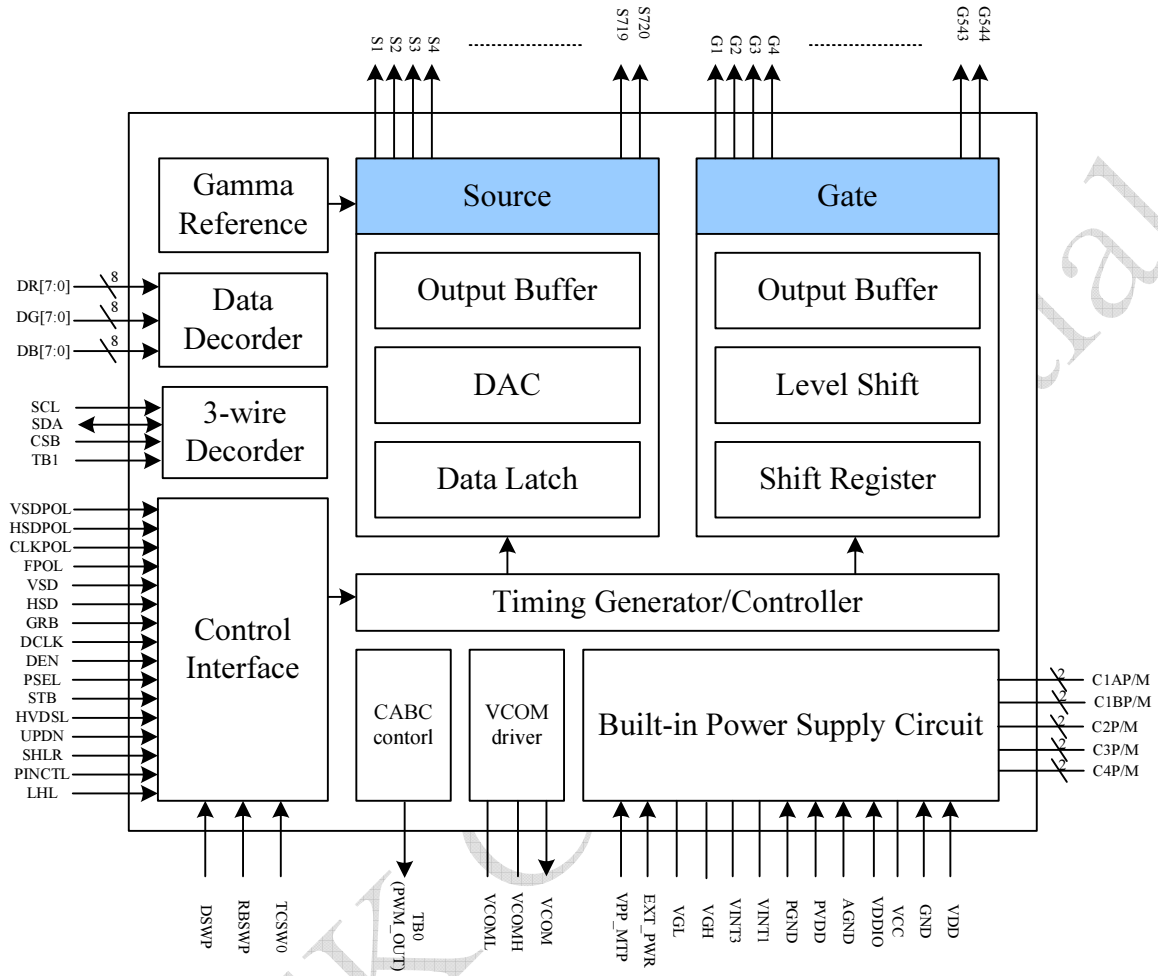
1. Introduction

The ILI6482C is a one-chip solution for a-TFT LCD panel focused on the resolution of 480[RGB] x 272. It integrates source driver, gate driver, built-in power generator, and timing controller in a single chip. The serial communication interface is also implemented for the register setting. For “Dual Gate Driver” panel application, the number of gate output is designed 544 channels to reduce the number of source output from 1440 to 720 channels in the ILI6482. This chip provides a real 8-bit resolution for 256-gray scales with a small deviation in source output to support a higher color resolution. Finally, the line inversion driving technique is also adopted in this chip for the lower-power dissipation concern.

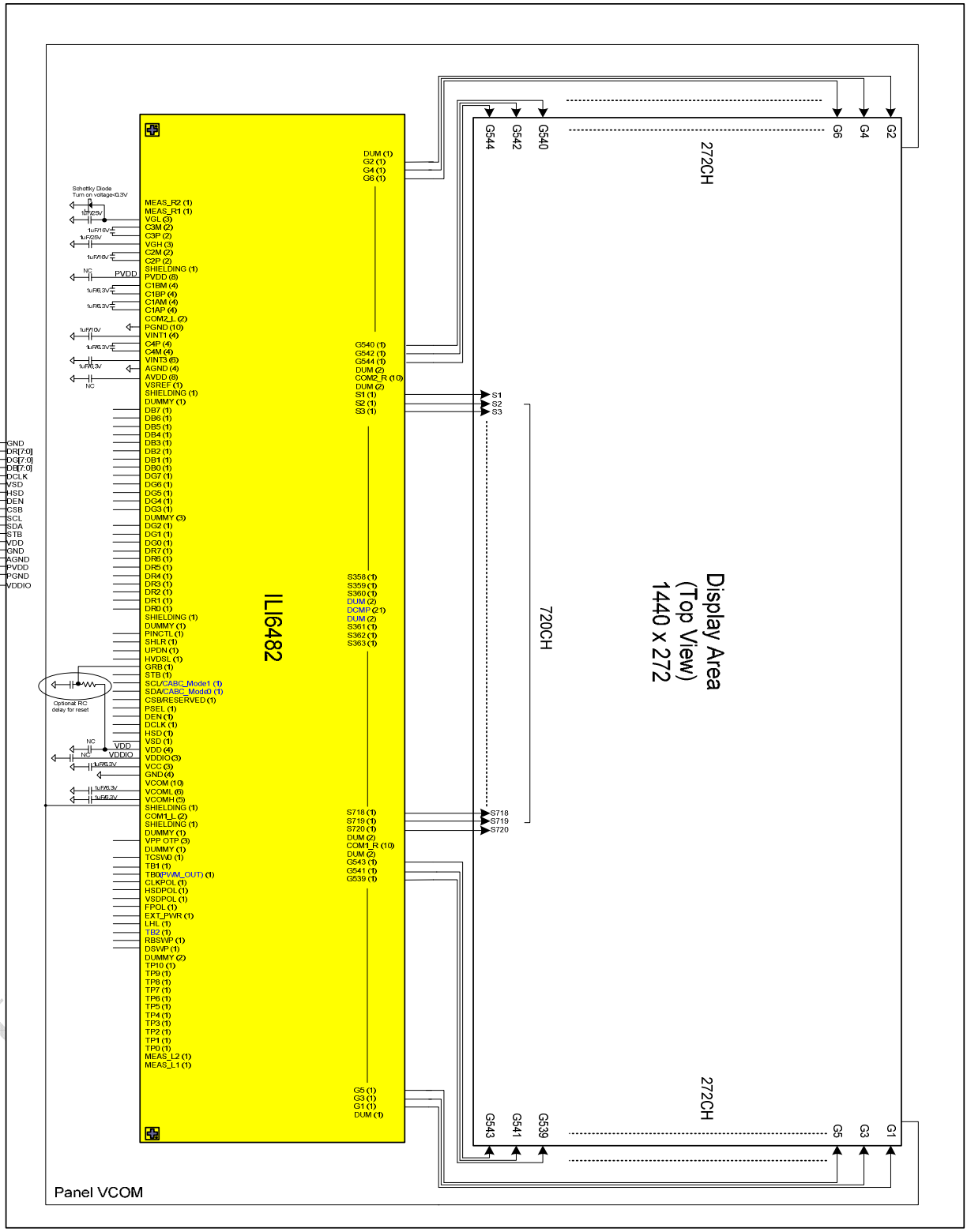
2. Features

- Generate 720 x 544 TFT control signals with timing controller.
- Panel resolution (HxV): 480[RGB] x 272.
- Source output with a real 8-bit resolution for 256 gray scales.
- Display function selected by 3-wire serial communication control.
- Build-in DC/DC charge pump, regulator, and VCOM are adjustable.
- Small source output deviation within ±20mV.
- Line inversion or half-line inversion is selectable.
- Right/Left shift function for source and Up/Down scan function for gate are selectable.
- Support to configure CABC block via 3-wire serial interface for LED backlight.
- Power for digital circuit (VDD): 3.0V ~ 3.6V.
- Power for analog circuit (PVDD): 3.0V ~ 3.6V.
- Power for interface (VDDIO): 1.8V ~ VDD.

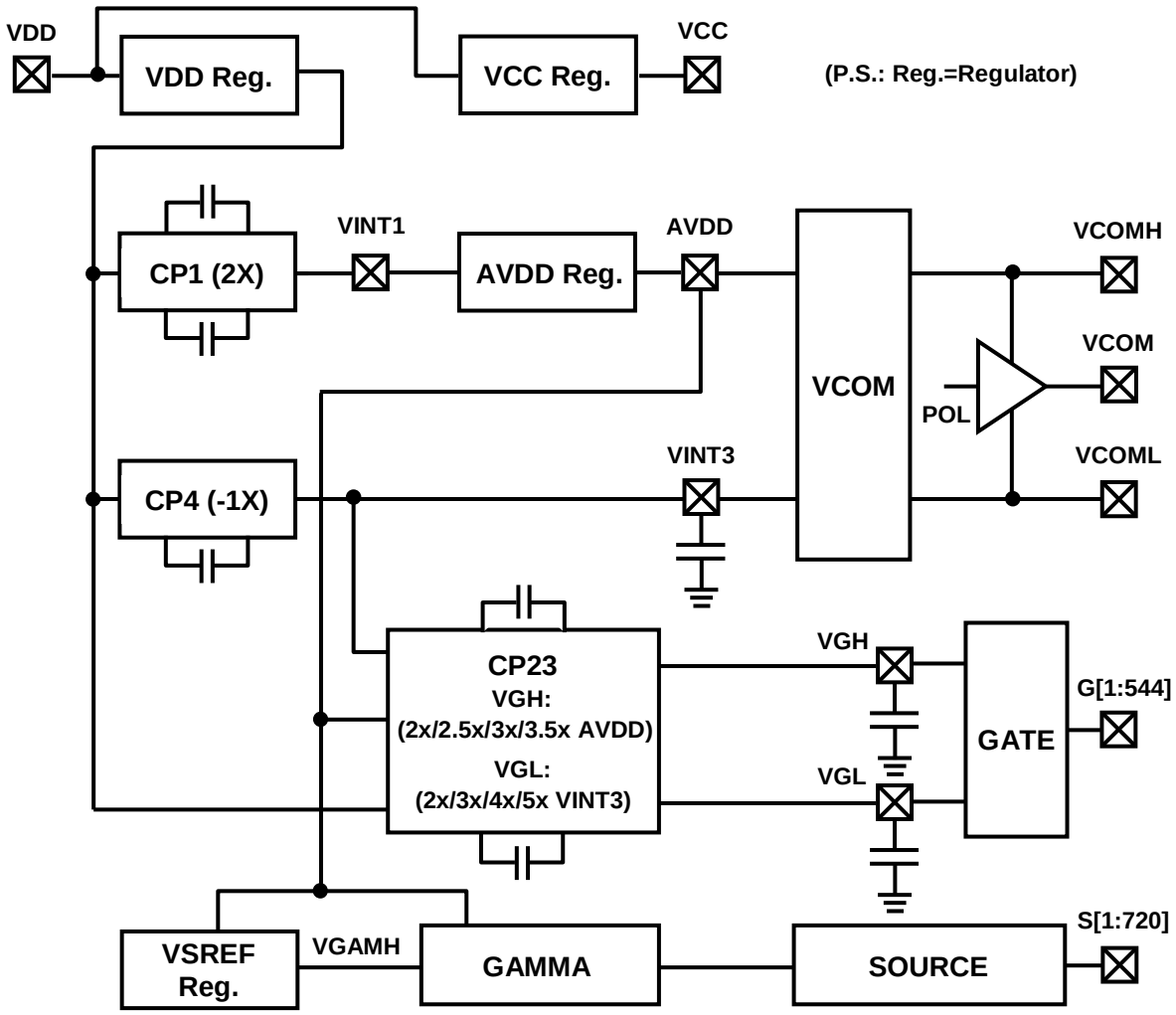
3. Block Diagram



4. Application Block

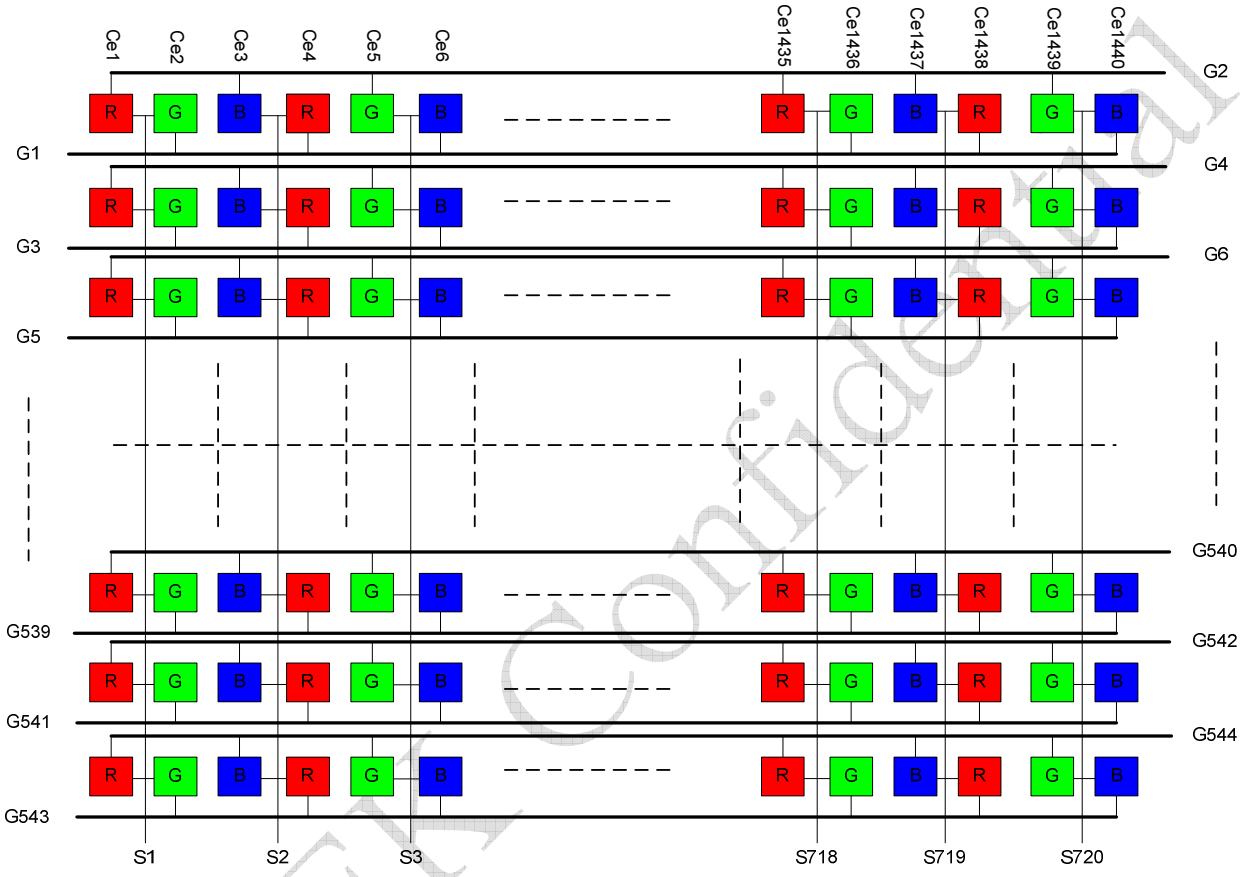


5. Charge Pump Circuit Block



6. Color Filter Arrangement

The ILI6482 supports the stripe color filter of dual-gate application. The color filter arrangement on panel is shown below.



7. Pin Descriptions

Pin Name	I/O	Descriptions
HSD	I (VDDIO)	Horizontal sync input. Negative polarity. ***Remark: Internal pulled weak high.**
VSD	I (VDDIO)	Vertical sync input. Negative polarity.. ***Remark: Internal pulled weak high.**
DCLK	I (VDDIO)	Dot clock signal input. Latching input data at its rising edge.
DEN	I (VDDIO)	Data enable input. Active high to enable the input data bus under “DE Mode.” ***Remark: Internal pulled weak low.**
PSEL	I (VDDIO)	Parallel 24-bit or serial 8-bit data input selection. PSEL=“H,” => Parallel 24-bit RGB input through DR[7:0], DG[7:0], and DB[7:0]. PSEL=“L,” => Serial 8-bit data input through DR[7:0]. ***Remark: Internal pulled weak high.**
DR[7:0]	I (VDDIO)	When PSEL=“H,” DR[7:0] will be treated as parallel 8-bit data input. When PSEL=“L,” DR[7:0] will be treated as serial 8-bit data input. ***Remark: Internal pulled weak low.**
DG[7:0]	I (VDDIO)	8-bit digital Green data input. DG[7:0] is only valid as PSEL= “H” (Parallel mode). ***Remark: Internal pulled weak low.**
DB[7:0]	I (VDDIO)	8-bit digital Blue data input. DB[7:0] is only valid as PSEL= “H” (Parallel mode). ***Remark: Internal pulled weak low.**
CSB	I (VDDIO)	Multi function control pin. When TB1=“L,” this pin acts as 3-wire “CSB” pin. When TB1=“H,” this pin is reserved. *** Remark: Internal pulled weak high.**
SDA	I/O (VDDIO)	Multi function control pin. When TB1=“L,” this pin acts as 3-wire “SDA” pin. When TB1=“H,” this pin acts as CABC mode select pin, CABCM[0] (LSB of CABCM). *** Remark: Internal pulled weak low**
SCL	I (VDDIO)	Multi function control pin. When TB1=“L,” this pin act as 3-wire “SCL” pin. When TB1=“H,” this pin act as CABC mode select pin, CABCM[1] (MSB of CABCM). CABCM[1:0] = 00b, OFF (Default) CABCM[1:0] = 01b, user interface image (in UI mode) CABCM[1:0] = 10b, still picture (in STILL mode) CABCM[1:0] = 11b, moving image (in MOV mode) ***Remark: Internal pulled weak low.**
STB	I (VDDIO)	Standby setting pin for testing. STB should be connected to VDDIO in normal operation mode. If STB is connected to GND, the IC is in standby mode. ***Remark: Internal pulled weak high.**
GRB	I (VDDIO)	Global reset pin. GRB should be connected to VDDIO in normal operating mode. If GRB is connected to GND, the timing controller is in reset state. It is suggested to be connected with a RC reset circuit for stability. ***Remark: Internal pulled weak high.**
HVDSL	I (VDDIO)	HV mode or DE mode control signal. HVDSL=“H” => Set under HV mode, VSD and HSD signals must be provided by system. HVDSL=“L” => Set under DE mode, and DEN signal must be provided by system. ***Remark: Internal pulled weak low.**
UPDN	I (VDDIO)	Up/Down scan control for gate driver. UPDN=“H” => Shift from up to down: L1 (The 1st line)->L2-> … ->L543->L544 (The last line). UPDN=“L” => Shift from down to up: L544 (The 1st line)->L543-> … ->L2->L1 (The last line). ***Remark: Internal pulled weak high.**

Pin Name	I/O	Descriptions
SHLR	I (VDDIO)	Right/Left sequence control for source driver. SHLR="H" => Shift to right: S1 (The 1st data)->S2->S3 … ->S720 (The last data). SHLR="L" => Shift to left: S1 (The last data) <-S2<-S3 … <-S720 (The 1st data). ***Remark: Internal pulled weak high.**
TB0 (PWM_OUT)	O (VDDIO)	PWM output control signal for CABC function.
TB1	I (VDDIO)	CABC/3-wire selection pin. TB1="H" => Select CABC hardware control function. TB1="L" => Select 3-wire SPI interface function. ***Remark: Internal pulled weak low.**
PINCTL	I (VDDIO)	Enable pin control function. PINCTL="H" => Enable pin control function. PINCTL="L" => Disable pin control function. ***Remark: Internal pulled weak low.** **Note: The 3-wire related control register will be disabled under PINCTL="H."**
EXT_PWR	I (VDDIO)	External power control pin. EXT_PWR="H" => Power could be input externally. EXT_PWR="L" => Power is generated by charge pump circuit. ***Remark: Internal pulled weak low.**
VSDPOL	I (VDDIO)	VSD polarity control pin. VSDPOL="H" => VSD actives in positive polarity. VSDPOL="L" => VSD actives in negative polarity. ***Remark: Internal pulled weak low.**
HSDPOL	I (VDDIO)	HSD polarity control pin. VSDPOL="H" => HSD actives in positive polarity. VSDPOL="L" => HSD actives in negative polarity. ***Remark: Internal pulled weak low.**
CLKPOL	I (VDDIO)	DCLK polarity control pin. CLKPOL="H" => Data are latched at DCLK falling edge. CLKPOL="L" => Data are latched at DCLK rising edge. ***Remark: Internal pulled weak low.**
FPOL	I (VDDIO)	VCOM polarity inverse control pin. When FPOL="H," VCOM works in normal polarity. When FPOL="L," the polarity of VCOM would be inversed during normal operation. ***Remark: Internal pulled weak high.**
LHL	I (VDDIO)	Line/Half-Line inversion control pin. LHL="H" => Half line inversion. LHL="L" => Line inversion. ***Remark: Internal pulled weak high.**
VDD	P	Power supply for digital circuits.
GND	P	Ground for digital circuits.
PVDD	P	Power supply for analog circuits.
PGND	P	Ground pin for power circuits.
AGND	P	Ground pin for analog circuits.
VDDIO	P	Power supply for logic I/O.
VPP_OTP	P	Customer OTP power input pin. **Note: If VPP_OTP is no use, please float this pin.**
VCC	C	Capacitor connect pin for internal regulator.
AVDD	I/O (Option)	Test pin for moniting VINT1 only.
VINT1	C	The capacitor connect pin for power setting.
VINT3	C	The capacitor connect pin for power setting.
VGH	C	The capacitor connect pin for power setting.
VGL	C	The capacitor connect pin for power setting.

C1AP/M C1BP/M C2P/M C3P/M C4P/M	C	Capacitor connect pin for internal charge pump. Refer to the section of “Power Circuit” for the application.
VCOM	O	The output pin for COMMON plate on panel.
VCOMH	C	The capacitor connect pin for the stable of the high-level VCOM output.
VCOML	C	The capacitor connect pin for the stable of the low-level VCOM output.
S720 ~ 1	O	The pin for source driver output signal.
G544 ~ 1	O	The pin for gate driver output signal.
DCMP	T	Test Pin. Please let this pin open.
ALIGN_R ALIGN_L	M	For assembly alignment.
COM1_L COM1_R	S	The internal COM1 linked together between input side and output side.
COM2_L COM2_R	S	The internal COM2 linked together between input side and output side.
DSWP	I	Data sequence control pin. When DSWP=“H,” data sequence is swapped. (DATA[7:0]=>DATA[0:7]) When DSWP=“L,” data sequence is normal. ***Remark: Internal pulled weak low.**
RBSWP	I	Red/Blue data swap control pin. When RBSWP=“H,” Red/Blue data are swapped (R→B and B→R). When RBSWP=“L,” Red/Blue data are not swapped. ***Remark: Internal pulled weak low.**
TP[9:0]	T	Test pins for internal testing only. ***Remark: No output connection.**
TP10	T	Test pin for internal testing only. ***Remark: No output connection and internal pulled weak low.**
TCSW0	I (VDDIO)	Enable pin control funciotn. As TCSW0=0, the VCOM frequency is splitted. As TCSW0=1, the VCOM frequency is fixed. ***Remark: Internal pulled weak low.**
TB2	T	Gate scan select function. TB2=“H,” Scan method 1. TB2=“L,” Scan method 2. ***Remark: Internal pulled weak low.**
SHIELDING	S	This pin is internal floating. ***Remark: No connection.**
DUM	D	Dummy pads. Leave this pin to be open.
DUMMY	D	Dummy pads. Leave this pin to be open
VSREF	T	Test pin for internal testing only. ***Remark: No connection**

Note:

I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, T: Testing, I/O: Input / Output, and C: Capacitor pin.

Pass Line Description:

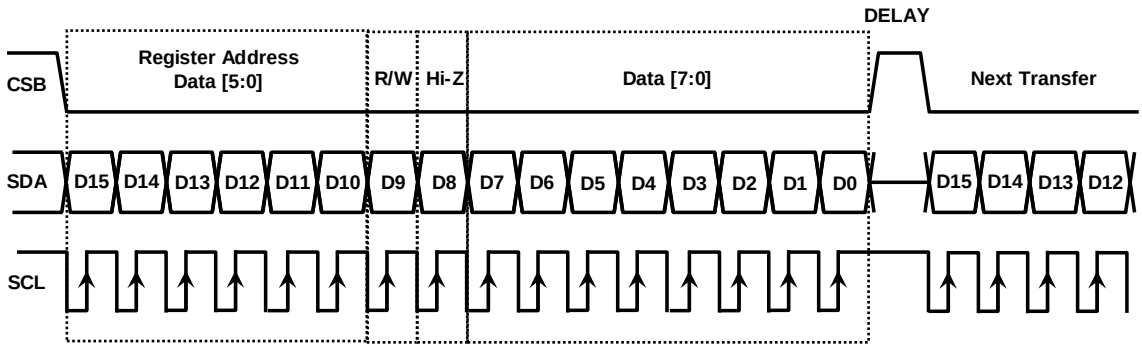
Pass Line no.	Pad Name	
1	COM1_L	COM1_R
2	COM2_L	COM2_R

8. 3-wire Serial Interface

The ILI6482 uses the 3-wire serial interface to set all the function and register parameter. The 3-wire serial interface is bi-directional and controlled by the R/W bit.

In the read mode, 3-wire serial interface will return the read data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored. During read operation, external controller should float SDA pin under the “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit to prevent from incorrect setting of the internal register; any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-wire serial
Interface.



Bit	Description
D[15:10]	Register Address Data [5:0].
D9	Write/Read (W/R) control bit. “0” for write and “1” for read.
D8	Any data within this bit will be ignored during write mode.
D[7:0]	Data for the W/R operation to the register address depend on address phase.

Note: Setting of all the registers will take effect at the coming falling edge of VSD signal except RESETB and STBYB bit.

9. Register List

N0	Address						R/W	D8	Parameter Data							
	D15	D14	D13	D12	D11	D10	D9		D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	R/W	x	HSDPOL	VSDPOL	CLKPOL	FPOL	NFSEL	FRAD1	FRAD0	DAT_INV
							1/0		0	0	0	0	0	0	0	0
R1	0	0	0	0	0	1	R/W	x	CABC_ MODE1	CABC_ MODE0	X	LHL	STB	GRB	SHRL	UPDN
							1/0		0	0	X	1	1	1	1	1
R4	0	0	0	1	0	0	R/W	x	DDL[7:0]							
							1/0		0	0	1	0	1	0	0	0
R5	0	0	0	1	0	1	R/W	x	X	X	X	HDL[4:0]				
							1/0		X	X	X	0	1	0	0	0
R6	0	0	0	1	1	0	R/W	x	VCOMH_OTP	VCOMH [6]	VCOMH [5]	VCOMH [4]	VCOMH [3]	VCOMH [2]	VCOMH [1]	VCOMH [0]
							1/0		0	1	0	0	0	0	1	1
R7	0	0	0	1	1	1	R/W	x	VCOML_OTP	VCOML [6]	VCOML [5]	VCOML [4]	VCOML [3]	VCOML [2]	VCOML [1]	VCOML [0]
							1/0		0	0	0	1	0	0	0	1
R8	0	0	1	0	0	0	R/W	x	BRI[7:0]							
							1/0		0	1	0	0	0	0	0	0
R9	0	0	1	0	0	1	R/W	x	CON_B[7:0]							
							1/0		0	1	0	0	0	0	0	0
R10	0	0	1	0	1	0	R/W	x	X	SUB_BRI_R[6:0]						
							1/0		X	1	0	0	0	0	0	0
R11	0	0	1	0	1	1	R/W	x	X	SUB_CON_R[6:0]						
							1/0		X	1	0	0	0	0	0	0
R12	0	0	1	1	0	0	R/W	x	X	SUB_BRI_B[6:0]						
							1/0		X	1	0	0	0	0	0	0
R13	0	0	1	1	0	1	R/W	x	X	SUB_CON_B[6:0]						
							1/0		X	1	0	0	0	0	0	0
R14	0	0	1	1	1	0	R/W	x	CABC_ BRI1	CABC_ BRI0	V2GAM[3:0]				GAMEN	x
							1/0		0	1	1	0	0	0	1	x
R15	0	0	1	1	1	1	R/W	x	V4GAM[3:0]				V3GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R16	0	1	0	0	0	0	R/W	x	V6GAM[3:0]				V5GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R17	0	1	0	0	0	1	R/W	x	V8GAM[3:0]				V7GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R18	0	1	0	0	1	0	R/W	x	X	X	X	X	V9GAM[3:0]			
							1/0		X	X	X	X	1	0	0	0
R19	0	1	0	0	1	1	R/W	x	X	X	VGH_OTP	VGH_SEL[1:0]		VGL_OTP	VGL_SEL[1:0]	
							1/0		X	X	0	1	1	0	0	1
R20	0	1	0	1	0	0	R/W	x	TRMEN[7:0]							
							1/0		0	0	0	0	0	0	0	0
R21	0	1	0	1	0	1	R/W	x	V13GAM[3:0]				V12GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R22	0	1	0	1	1	0	R/W	x	V15GAM[3:0]				V14GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R23	0	1	0	1	1	1	R/W	x	V17GAM[3:0]				V16GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R24	0	1	1	0	0	0	R/W	x	V19GAM[3:0]				V18GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R30	0	1	1	1	1	0	W	x	DBV[7:0]							
							0		1	1	1	1	1	1	1	1
R31	0	1	1	1	1	1	R	x	DBV[7:0]							
							1	x	1	1	1	1	1	1	1	1
R32	1	0	0	0	0	0	W	x	X	X	BCTL	X	DD	BL	X	X
							0		X	X	1	X	1	1	X	X

R33	1	0	0	0	0	1	R	x	X	X	BCTL	X	DD	BL	X	X
							1		X	X	1	X	1	1	X	X
R36	1	0	0	1	0	0	W	x	CMB[7:0]							
							0		0	0	0	0	0	0	0	0
R37	1	0	0	1	0	1	R	x	CMB[7:0]							
							1		0	0	0	0	0	0	0	0
R38	1	0	0	1	1	0	W	x	PWM_DIV[7:0]							
							0		0	0	0	0	1	1	1	1
R39	1	0	0	1	1	1	W	x	THRES_MOV[3:0]				THRES_STILL[3:0]			
							0		1	0	1	1	1	0	1	1
R40	1	0	1	0	0	0	W	x	X	X	X	X	THRES_UI[3:0]			
							0		X	X	X	X	1	0	1	1
R41	1	0	1	0	0	1	W	x	Min-DTH_MOV[3:0]				Min-DTH_STILL[3:0]			
							0		1	0	1	0	1	0	0	0
R42	1	0	1	0	1	0	W	x	X	X	X	X	Min-DTH_UI[3:0]			
							0		X	X	X	X	0	1	0	0
R43	1	0	1	0	1	1	W	x	X	DIM_MOV[2:0]			X	DIM_STILL[2:0]		
							0		X	1	0	0	X	0	1	1
R44	1	0	1	1	0	0	W	x	DIM_MIN[3:0]				X	DIM_UI[2:0]		
							0		0	0	0	0	X	0	1	0
R45	1	0	1	1	0	1	W	x	X	X	X	X	X	LEDONR	LEDONPOL	PWMPOL
							0		X	X	X	X	X	0	0	0

Register R0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HSDPOL	VSDPOL	CLKPOL	FPOL	NFSEL	FRAD1	FRAD0	DAT_INV
Default	0	0	0	0	0	0	0	0

DAT_INV: Source output inversion control.

DAT_INV="0": Data output normal. (Default)

DAT_INV="1": Data output inversion.

FRAD[1:0]: Odd / Even frame advance control. FRAD should be correctly configured if the incoming data of HBP in even-frame and that of odd-frame are different. There are three examples for FRAD setting reference.

Example 1: If HBP in odd-frame is 21 and HBP in even-frame is 21, FRAD should be set to 0 and HDL should be set to 21.

Example 2: If HBP in odd-frame is 21 and HBP in even-frame is 22 (odd frame advance), FRAD should be set to 1 and HDL should be set to 21.

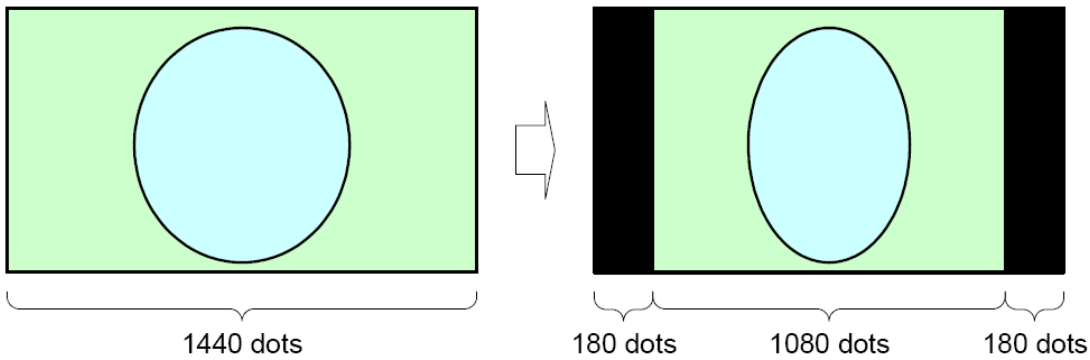
Example 3: If HBP in odd-frame is 21 and HBP in even-frame is 20 (even frame advance), FRAD should be set to 2 and HDL should be set to 20.

FRAD1	FRAD0	Descriptions	Notes
0	0	Default	Odd/Even frame Tstv are the same
0	1	Odd frame advance	Even frame Tstv = HDL setting +1
1	0	Even frame advance	Odd frame Tstv = HDL setting +1
1	1	Reserved	Reserved

NFSEL: Narrow display mode selection.

NFSEL="1": Narrow display format is enabled.

NFSEL="0": Normal display is selected. (Default)



FPOL: VCOM polarity inverse control.

FPOL="0": VCOM works in inverse polarity.

FPOL="1": VCOM works in normal polarity. (Default)

CLKPOL: DCLK polarity control.

CLKPOL="1": Data are latched at DCLK falling edge.

CLKPOL="0": Data are latched at DCLK rising edge. (Default)

VSDPOL: VSD polarity control.

VSDPOL="1": VSD actives in positive polarity.

VSDPOL="0": VSD actives in negative polarity. (Default)

HSDPOL: HSD polarity control.

HSDPOL="1": HSD actives in positive polarity.

HSDPOL="0": HSD actives in negative polarity. (Default)

Register R1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CABC_MODE[1]	CABC_MODE[0]	x	LHL	STB	GRB	SHRL	UPDN
Default	0	0		1	1	1	1	1

UPDN: Control the Up/Down scan direction for the gate driver.

UPDN="1" => Gate signal shift from-Up-to-Down: L1 (The first line) → L2 → … → L543 → L544 (The last line) (Default)

UPDN="0" => Gate signal shift from-Down-to-Up: L544 (The first line) → L543 → … → L2 → L1 (The last line)

SHRL: Control the Right/Left sequence for the source driver.

SHLR="1" => Shift from Right: S1 (The first data) → S2 → S3 … → S720 (The last data). (Default)

SHLR="0" => Shift from Left: S1 (The last data) ← S2 ← S3 … ← S720 (The first data).

GRB: Global reset bit.

GRB="1" => Normal operation. (Default)

GRB="0" => Reset state.

STB: Standby mode selection bit.

STB="1" => Normal operation. (Default)

STB="0" => Standby mode.

LHL: Line/Half-Line inversion selection bit.

LHL="1" => Half line inversion. (Default)

LHL="0" => Line inversion.

CABC_MODE[1:0]: CABC operation mode selection.

CABC_MODE[1:0]	Description
2'b00	CABC OFF (Default)
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Register R4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DDL[7:0]							
Default	0	0	1	0	1	0	0	0

DDL[7:0]: Select the delay time of the HSD signal to the first input data coming.

DDL[7:0]	DDL Function	UNIT
8'h00	Setting prohibited	DCLK
8'h01	Setting prohibited	
…	…	
8'h24	Setting prohibited	
8'h25	37	
8'h26	38	
…	…	
8'h28	40(Default setting for Parallel mode)	
8'h29	41	
…	…	
8'h78	120(Default setting for Serial mode)	
8'h79	121	
…	…	
8'hFF	255	

Register R5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	X	HDL[4:0]				
Default	x	x	X	0	1	0	0	0

(X: Don't care)

HDL[4:0]: Select the output delay time of the gate start pulse.

HDL[4:0]	HDL Function	UNIT
5'h00	Setting prohibited	HSD
…	…	
5'h05	5	
…	…	
5'h08	8 (default)	
…	…	
5'h1F	31	

Register R6

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOMH_OTP	VCOMH[6]	VCOMH[5]	VCOMH[4]	VCOMH[3]	VCOMH[2]	VCOMH[1]	VCOMH[0]
Default	0	1	0	0	0	0	1	1

VCOMH[6:0]: Set the VCOMH voltage with a 20mV/LSB.

VCOMH[6:0]	VCOMH Voltage	Unit
7'b00h	2.46	Volt
7'b01h	2.48	
…	…	
7'b1Bh	3	
7'b1Ch	3.02	
…	…	
7'b4Dh	4.00(default)	
7'b4Eh	4.02	
…	…	
7'b7Fh	5	

Note: To prevent device damage, please follow VCOMH-VCOML<6.2V.

VCOMH_OTP:

As VCOMH_OTP ="1," VCOMH is switched to the 3-wire register memory.

As VCOMH_OTP ="0," VCOMH is read from OTP memory. (Default)

Register R7

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOML_OTP	VCOML[6]	VCOML[5]	VCOML[4]	VCOML[3]	VCOML[2]	VCOML[1]	VCOML[0]
Default	0	0	0	1	0	0	0	1

VCOML[6:0]: Set the VCOML voltage with a 20mV/LSB.

VCOML[6:0]	VCOML Voltage	Unit
7'b00h	-0.46	Volt
7'b01h	-0.48	
…	…	
7'b27h	-1.24	
7'b28h	-1.26(default)	
…	…	
7'b4Dh	-2	
7'b4Eh	-2.02	
…	…	
7'b7Fh	-3	

Note: Please follow VCOMH-VCOML<6.2V to prevent device damage.

VCOML_OTP:

As VCOML_OTP ="1," VCOML is switched to the 3-wire register memory.

As VCOML_OTP ="0," VCOML is read from OTP memory. (Default)

Register R8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BRI[7:0]							
Default	0	1	0	0	0	0	0	0

BRI[7:0]: Brightness level setting; the gain changes with 1 step/bit.

BRI[7:0]	Brightness Offset
8'h00	Dark (-64)
8'h01	-63
…	…
8'h40	Center (0, Default)
…	…
8'hFF	Bright (+191)

Register R9

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CON[7:0]							
Default	0	1	0	0	0	0	0	0

CON[7:0]: Contrast level setting; the gain changes with (1/64)/bit.

CON[7:0]	Contrast Gain
8'h00	0
8'h01	1/64
…	…
8'h40	1 (Default)
…	…
8'hFF	3.984

Register R10

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	SUB_BRI_R[6:0]						
Default	x	1	0	0	0	0	0	0

(X: Don't care)

SUB_BRI_R[6:0]: The setting for Red sub-pixel brightness level; the setting accuracy is 1 step/bit.

SUB_BRI_R[6:0]	Red Brightness Offset
7'h00	Dark (-64)
7'h01	-63
…	…
7'h40	Center (0) (Default)
…	…
7'h7F	Bright (+63)

Register R11

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	SUB_CON_R[6:0]						
Default	x	1	0	0	0	0	0	0

(X: Don't care)

SUB_CON_R[6:0]: The setting for Red sub-pixel contrast level; the gain changes with (1/256)/bit.

SUB_CON_R[6:0]	Red Contrast Gain
7'h00	0.75
7'h01	0.75+ 1/256
…	…
7'h40	1 (Default)
…	…
7'h7F	1.246

Register R12

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	SUB_BRI_B[6:0]						
Default	x	1	0	0	0	0	0	0

(X: Don't care)

SUB_ BRI _B[6:0]: The setting for Blue sub-pixel brightness level; the setting accuracy is 1 step/bit.

SUB_BRI_B[6:0]	Blue Brightness Offset
7'h00	Dark (-64)
7'h01	-63
…	…
7'h40	Center (0) (Default)
…	…
7'h7F	Bright (+63)

Register R13

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	SUB_CON_B[6:0]						
Default	x	1	0	0	0	0	0	0

(X: Don't care)

SUB_CON_B[6:0]: The setting for Blue sub-pixel contrast level; the gain changes with (1/256)/bit.

SUB_CON_B[6:0]	Blue Contrast Gain
7'h00	0.75
7'h01	0.75+ 1/256
…	…
7'h40	1 (Default)
…	…
7'h7F	1.246

Register R14

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CABC_BRI1	CABC_BRI0	V2GAM[3:0]				GAMEN	x
Default	0	1	1	0	0	0	1	x

(X: Don't care)

GAMEN: The control bit for GAMMA correction. (V2-V9 and V12-V19 GAMMA voltage levels)

GAMEN="1," Gamma correction enabled. (Default)

GAMEN="0," Gamma correction disabled.

V2GAM[3:0]: V2 GAMMA voltage level setting. Adjust level = 20mV / Step.

CABC_BRI[1:0]: CABC brightness level selection.

CABC_BRI[1:0]	Brightness level
2'b00	Low level
2'b01	Normal level (Default)
2'b10	High level
2'b11	Higher level

Register R15

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V4GAM[3:0]				V3GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V3GAM[3:0]: V3 GAMMA voltage level setting. Adjust level = 20mV / Step.

V4GAM[3:0]: V4 GAMMA voltage level setting. Adjust level = 20mV / Step.

Register R16

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V6GAM[3:0]				V5GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V5GAM[3:0]: V5 GAMMA voltage level setting. Adjust level = 20mV / Step.

V6GAM[3:0]: V6 GAMMA voltage level setting. Adjust level = 20mV / Step.

Register R17

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V8GAM[3:0]				V7GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V7GAM[3:0]: V7 GAMMA voltage level setting. Adjust level = 20mV / Step.

V8GAM[3:0]: V8 GAMMA voltage level setting. Adjust level = 20mV / Step.

Register R18

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	x	V9GAM[3:0]			
Default	x	x	x	x	1	0	0	0

(X: Don't care)

V9GAM[3:0]: V9 GAMMA voltage level setting. Adjust level = 20mV / Step.

VXGAM[3:0]	Gamma Voltage	Unit	Note
4'h0	+160	mV	Refer to the Gamma Table for the default voltage level of V2~V9
4'h8	VXGAM[3:0]		
4'hF	-140		

Register R19

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	VGH_OTP	VGH_SEL[1:0]		VGL_OTP	VGL_SEL[1:0]	
Default	x	x	0	1	0	0	0	1

(X: Don't care)

VGH_SEL[1:0]: VGH output voltage selection.

VGH_SEL[1:0]	VGH Voltage	Unit
2'b00	2×VINT1	Volt
2'b01	2.5×VINT1	
2'b10	3×VINT1 (default)	
2'b11	3.5×VINT1	

VGH_OTP:

As VGH_OTP = "1," VGH is switched to the 3-wire register memory.

As VGH_OTP = "0," VGH is read from OTP memory. (Default)

VGL_SEL[1:0]: VGL output voltage selection.

VGL_SEL[1:0]	VGL Voltage	Unit
2'b00	2×VINT3	Volt
2'b01	3×VINT3 (default)	
2'b10	4×VINT3	
2'b11	5×VINT3	

VGL_OTP:

VGL_OTP = "1," VGL is switched to the 3-wire register memory.

VGL_OTP = "0," VGL is read from OTP memory. (Default)

Register R20

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRMEN[7:0]							
Default	0	0	0	0	0	0	0	0

TRMEN[7:0]: Trimming function control register for VCOMH, VCOML, VGH, and VGL.

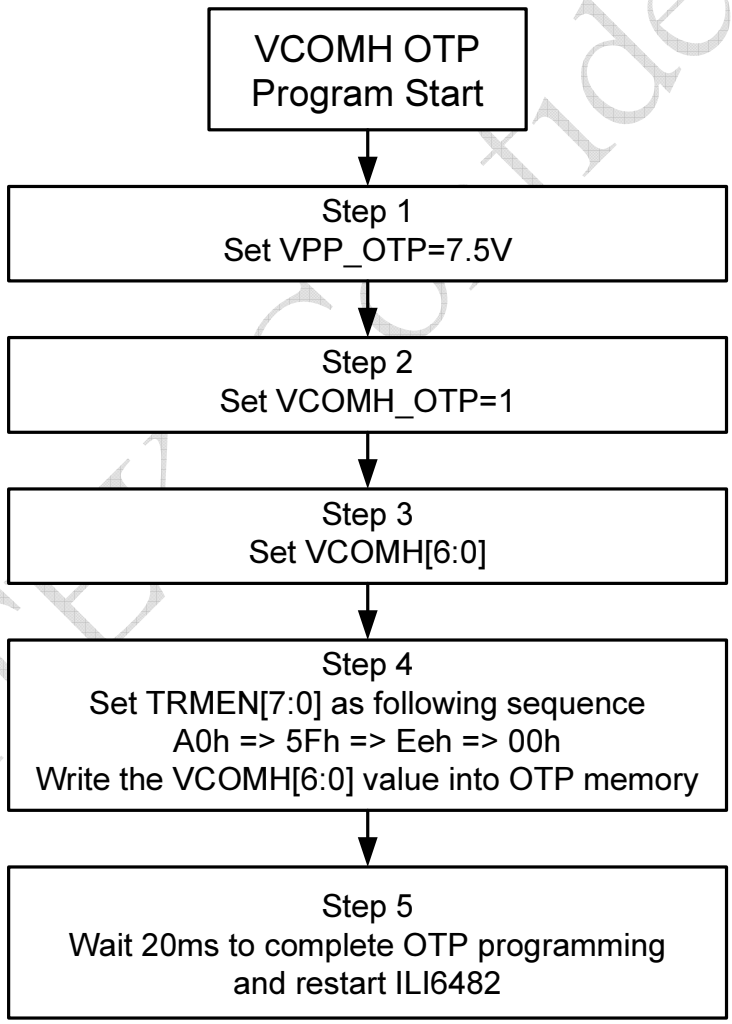
Sequentially write the following commands to enable VCOMH[6:0], VCOML[6:0], VGH_SEL[1:0], or VGL_SEL[1:0] trimming functions.

Take adjustung VCOMH level for example:

(1) Set TRMEN[7:0]=00H and write a proper VCOMH[6:0] value by the 3-wire SPI interface.

(2) Program the VCOMH[6:0] value into OTP memory.

(3) Set TRMEN[7:0] as following sequence: A0h->5Fh->EEh->00h.



Note:

1. **The trim block can be written 3 times for VCOMH/VCOML and 1 time for VGH/VGL.**
2. **Trim command exceeded the limit may cause the unknown values at VCOMH/VCOML/VGH/VGL output.**

Register R21

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V13GAM[3:0]				V12GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V12GAM[3:0]: V12 GAMMA voltage level setting. Adjust level = 20mV / Step.

V13GAM[3:0]: V13 GAMMA voltage level setting. Adjust level = 20mV / Step.

Register R22

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V15GAM[3:0]				V14GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V14GAM[3:0]: V14 GAMMA voltage level setting. Adjust level = 20mV / Step.

V15GAM[3:0]: V15 GAMMA voltage level setting. Adjust level = 20mV / Step.

Register R23

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V17GAM[3:0]				V16GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V16GAM[3:0]: V16 GAMMA voltage level setting. Adjust level = 20mV / Step.

V17GAM[3:0]: V17 GAMMA voltage level setting. Adjust level = 20mV / Step.

Register R24

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V19GAM[3:0]				V18GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V18GAM[3:0]: V18 GAMMA voltage level setting. Adjust level = 20mV / Step.

V19GAM[3:0]: V19 GAMMA voltage level setting. Adjust level = 20mV / Step.

Register R30 (Write Display Brightness Value)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DBV[7:0]							
Default	1	1	1	1	1	1	1	1

DBV[7:0]: This command is used to adjust the brightness value of display. The pulse duty of PWM_OUT signal is selected from 256 values between 8'hFF and 8'h00 to adjust the LED brightness.

When this register is read back, the LED brightness data for PWM_OUT signal are read by the baseband which can adjust the backlight brightness depending on the read back DBV values.

Register R31 (Read Display Brightness Value)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DBV[7:0]							
Default	1	1	1	1	1	1	1	1

This command is used to read the Display Brightness Value (DBV) register.

Register R32 (Write Display CTRL)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	BCTL	x	DD	BL	x	x
Default	x	x	1	x	1	1	x	x

(X: Don't care)

BCTRL: Brightness Control Block On/Off.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active) (Default)

DD: Display Dimming Control. This function is only for manual brightness setting. When the CABC is enabled, the dimming function is automatically controlled by CABC block.

DD	Description
0	Display Dimming OFF (Changes immediately)
1	Display Dimming On (Changes gradually base on the R43 register setting) (Default)

BL: Backlight Control (PWM_OUT signal) On/Off.

BL	Description
0	Backlight Control OFF
1	Backlight Control ON (Default)

When the BL bit changes from "On" to "Off", the backlight is turned off without gradual dimming even if the dimming-on (DD=1) is selected.

Register R33 (Read CTRL Display)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	BCTL	x	DD	BL	x	x
Default	x	x	1	x	1	1	x	x

(X: Don't care)

This command is used to read the CTRL register.

Register R36 (Write the Minimum CABC Brightness)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMB[7:0]							
Default	0	0	0	0	0	0	0	0

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: This register is used to limit the brightness reduction. When CABC function is enabled, the display brightness could not be reduced to exceed the minimum CABC brightness setting. However, if the CABC function is disabled, the minimum CABC brightness setting is ignored and user can set the value of DBV[7:0] smaller than that of CMB[7:0].

Register R37 (Read the Minimum CABC Brightness)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMB[7:0]							
Default	0	0	0	0	0	0	0	0

This command is used to read the minimum brightness value of the display for CABC function.

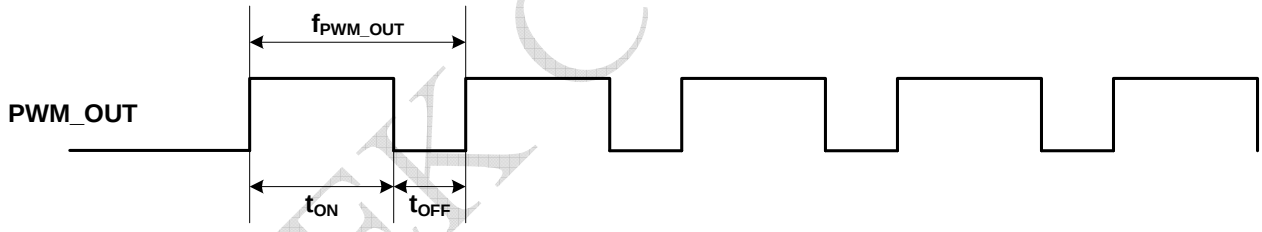
Register R38 (CABC Control 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWM_DIV[7:0]							
Default	0	0	0	0	1	1	1	1

PWM_DIV[7:0]: PWM_OUT output frequency control. The PWM_OUT frequency can be calculated by the following equation and the PWM_OUT duty is based on the CABC result.

$$f_{pwm\_out} = \frac{9MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

PWM_DIV[7:0]	f_{PWM_OUT}
8'h0	31.37 kHz
8'h1	15.69 kHz
8'h2	10.46 kHz
8'h3	7.843 kHz
…	…
8'hF	2.026 kHz (Default)
…	…
8'hFC	140Hz
8'hFD	139Hz
8'hFE	138Hz
8'hFF	137Hz



Note: The output frequency tolerance of internal frequency divider in CABC is ±10%.

Register R39 (CABC Control 2)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	THRES_MOV[3:0]				THRES_STILL[3:0]			
Default	1	0	1	1	1	0	1	1

THRES_MOV[3:0]: These bits are used to set the percentage of grayscale data accumulated in the histogram in the moving picture mode (MOV mode).

The description ratio is the maximum number of pixels that makes white-image display (Data = “255”) to the total of pixels under image processing.

THRES_MOV[3:0]	Description
4’h0	99%
4’h1	98%
4’h2	96%
4’h3	94%
4’h4	92%
4’h5	90%
4’h6	88%
4’h7	86%

THRES_MOV[3:0]	Description
4’h8	84%
4’h9	82%
4’hA	80%
4’hB	78%(Default)
4’hC	76%
4’hD	74%
4’hE	72%
4’hF	70%

THRES_STILL[3:0]: These bits are used to set the percentage of grayscale data accumulated in the histogram in the still picture mode (STILL mode).

The description ratio is the maximum number of pixels that makes white-image display (Data = “255”) to the total of pixels under image processing.

THRES_STILL[3:0]	Description
4’h0	99%
4’h1	98%
4’h2	96%
4’h3	94%
4’h4	92%
4’h5	90%
4’h6	88%
4’h7	86%

THRES_STILL[3:0]	Description
4’h8	84%
4’h9	82%
4’hA	80%
4’hB	78% (Default)
4’hC	76%
4’hD	74%
4’hE	72%
4’hF	70%

Register R40 (CABC Control 3)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	x	THRES_UI[3:0]			
Default	x	x	x	x	1	0	1	1

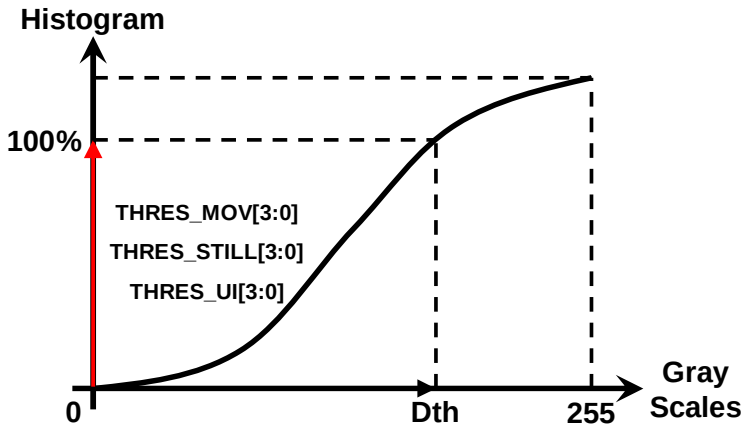
(X: Don't care)

THRES_UI[3:0]: These bits are used to set the percentage of grayscale data accumulated in the histogram in the user interface mode (UI mode).

The description ratio is the maximum number of pixels that makes white-image display (=data "255") to the total of pixels under image processing.

THRES_UI[3:0]	Description
4'h0	99%
4'h1	98%
4'h2	96%
4'h3	94%
4'h4	92%
4'h5	90%
4'h6	88%
4'h7	86%

THRES_UI[3:0]	Description
4'h8	84%
4'h9	82%
4'hA	80%
4'hB	78%(Default)
4'hC	76%
4'hD	74%
4'hE	72%
4'hF	70%



Register R41 (CABC Control 4)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Min-DTH_MOV[3:0]				Min-DTH_STILL[3:0]			
Default	1	0	1	0	1	0	0	0

Min-DTH_MOV[3:0]: This parameter is used set the minimum of grayscale threshold value the moving picture mode (MOV mode). The minimum Dth would be restricted to prevent too white display image whose qulity is not acceptable.

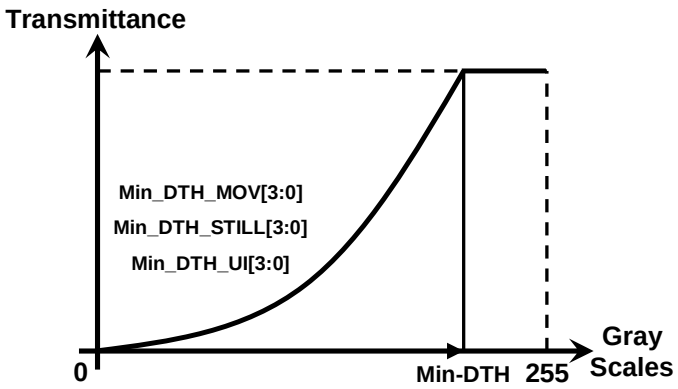
Min-DTH_MOV[3:0]	Description
4'h0	224
4'h1	220
4'h2	216
4'h3	212
4'h4	208
4'h5	204
4'h6	200
4'h7	196

Min-DTH_MOV[3:0]	Description
4'h8	192
4'h9	188
4'hA	184 (Default)
4'hB	180
4'hC	176
4'hD	172
4'hE	168
4'hF	164

Min-DTH_STILL[30]: This parameter is used set the minimum of grayscale threshold value in the still picture mode (STILL mode). The minimum Dth would be restricted to prevent too white display image whose qulity is not acceptable.

Min-DTH_STILL[3:0]	Description
4'h0	224
4'h1	220
4'h2	216
4'h3	212
4'h4	208
4'h5	204
4'h6	200
4'h7	196

Min-DTH_STILL[3:0]	Description
4'h8	192(Default)
4'h9	188
4'hA	184
4'hB	180
4'hC	176
4'hD	172
4'hE	168
4'hF	164



Register R42 (CABC Control 5)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	x	Min-DTH_UI[3:0]			
Default	x	x	x	x	0	1	0	0

(X: Don't care)

Min-DTH_UI[3:0]: This parameter is used set the minimum of grayscale threshold value in the user interface mode (UI mode). The minimum Dth would be restricted to prevent too white display image whose qulity is not acceptable.

Min-DTH_UI[3:0]	Description
4'h0	252
4'h1	248
4'h2	244
4'h3	240
4'h4	236 (Default)
4'h5	232
4'h6	228
4'h7	224

Min-DTH_UI[3:0]	Description
4'h8	220
4'h9	216
4'hA	212
4'hB	208
4'hC	204
4'hD	200
4'hE	196
4'hF	192

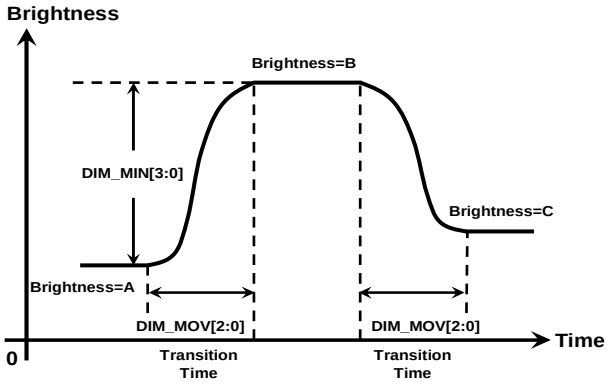
Register R43 (CABC Control 6)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	DIM_MOV[2:0]			x	DIM_STILL[2:0]		
Default	x	1	0	0	x	0	1	1

(X: Don't care)

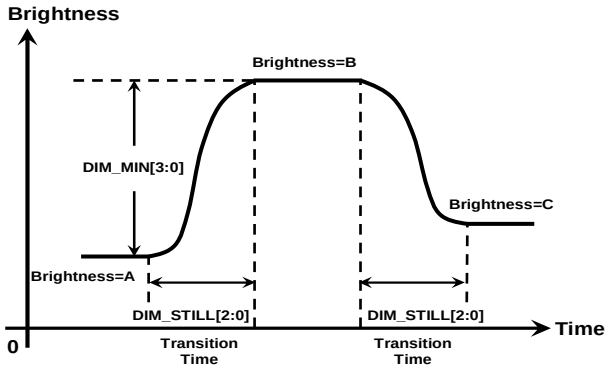
DIM_MOV[2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision in the MOV mode.

DIM_MOV[2:0]	Description
3'h0	1 frame
3'h1	1 frame
3'h2	2 frames
3'h3	4 frames
3'h4	8 frames(Default)
3'h5	16 frames
3'h6	32 frames
3'h7	64 frames



DIM_STILL[2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision in the STILL mode.

DIM_STILL[2:0]	Description
3'h0	1 frame
3'h1	1 frame
3'h2	2 frames
3'h3	4 frames(Default)
3'h4	8 frames
3'h5	16 frames
3'h6	32 frames
3'h7	64 frames



Register R44 (CABC Control 7)

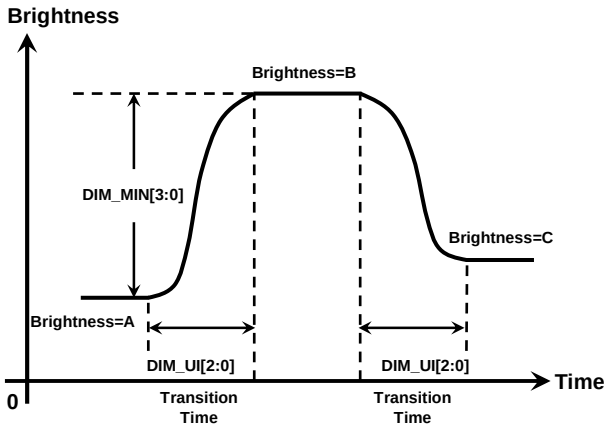
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIM_MIN[3:0]				x	DIM_UI[2:0]		
Default	0	0	0	0	x	0	1	0

(X: Don't care)

DIM_MIN[3:0]: The parameter is used to set the imitation of the minimum brightness change. The brightness will not change if the minimum brightness change per setp is larger than the difference between target brightness and current brightness.

DIM_UI[2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision in the UI mode.

DIM_UI[2:0]	Description
3'h0	1 frame
3'h1	1 frame
3'h2	2 frames(Default)
3'h3	4 frames
3'h4	8 frames
3'h5	16 frames
3'h6	32 frames
3'h7	64 frames



Register R45 (CABC Control 8)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	x	x	LEDONR	LEDONPOL	PWMPOL
Default	x	x	x	x	x	0	0	0

(X: Don't care)

LEDONR: This bit is used to control PWM_OUT pin.

LEDONR	Description
0	Low
1	High

LEDONPOL: This bit is used to control PWM_OUT pin.

BL	LEDONPOL	Description
0	0	0
0	1	1
1	0	LEDONR
1	1	Inversed LEDONR

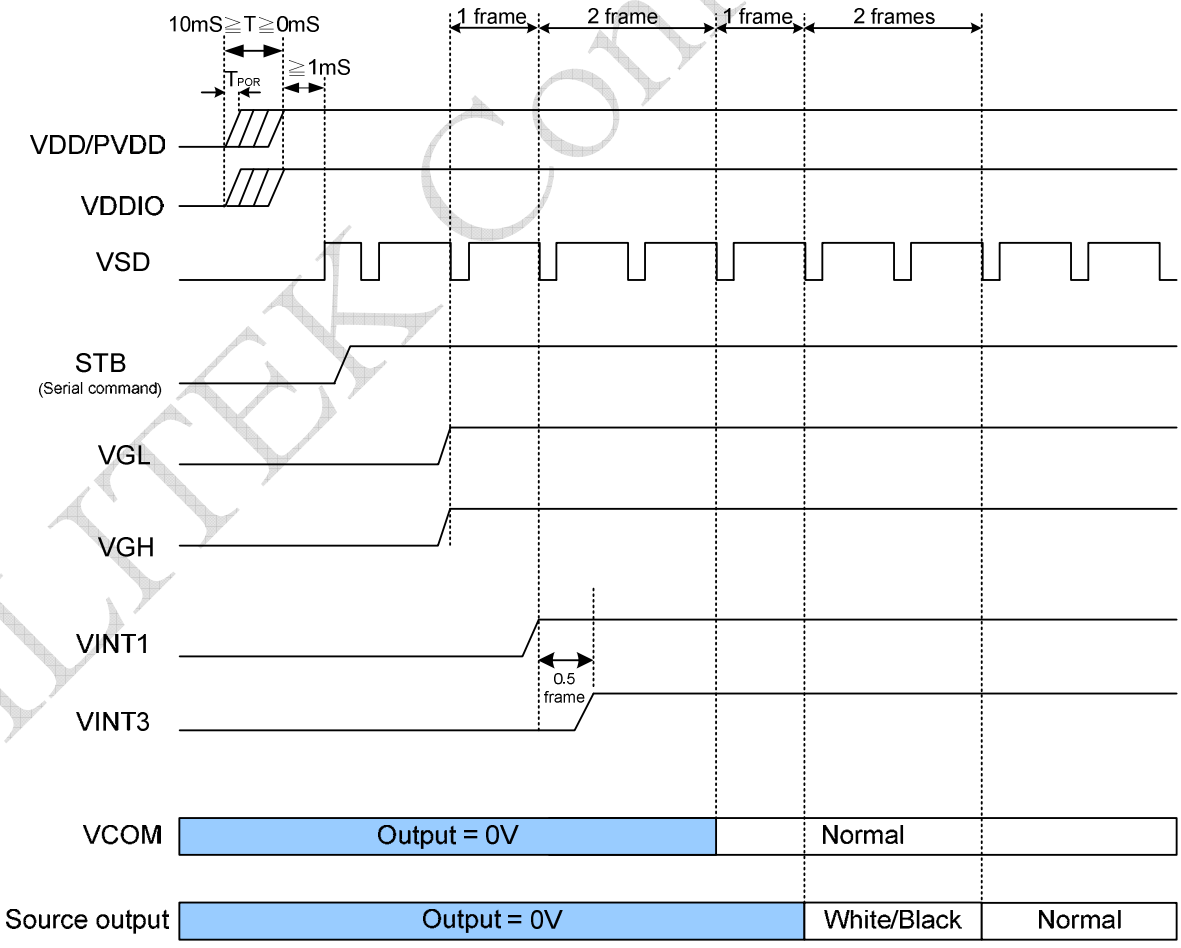
PWMPOL: The bit is used to define polarity of PWM_OUT signal.

BL	PWMPOL	Description
0	0	Always low
0	1	Always high
1	0	Original polarity of PWM_OUT signal
1	1	Inversed polarity of PWM_OUT signal

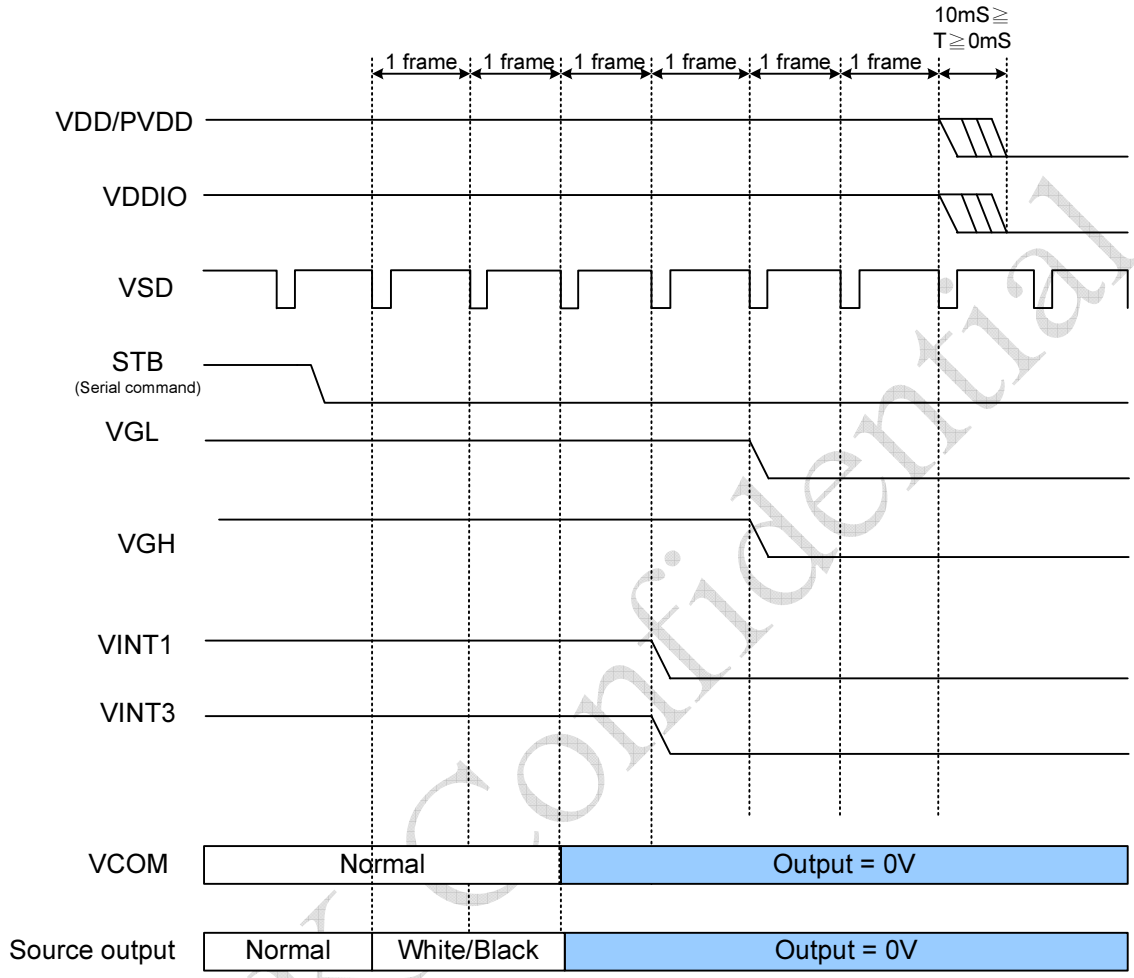
10. Power On/Off Sequence

Please follow the following recommended power on/off sequence to correctly turn on/off the ILI6482. VDD and PVDD are externally connected together on system. Starting into power-on sequence, VDD and VDDIO could be applied in any order wintin 10-ms duration. After VDD or VDDIO rises over 1ms, VSD would be valided after STB rises and then trigger on VGL and VGH behind 1 frame. Following, VINT1, VINT3, VCOM, and source output would be turned on sequentially, as shown in Fig. 10.1. On the contrary, Starting into power-off sequence, source output, VCOM, VINT1, and VINT3, are turened off in order after STB falls with one VSD turrend on, as shown in Fig. 10.2. After VGL is turned off over 2 frames, VDD and PVDD could be turned off in any order wintin 10-ms duration. By the way, if the external reset is used for power-on sequence, RSTB should go high after VDD or VDDIO rises over 1ms. The external reset is vailded only when the pulse duration of RSTB with a negative polarity is larger than 50us, as shown in Fig. 10.3.

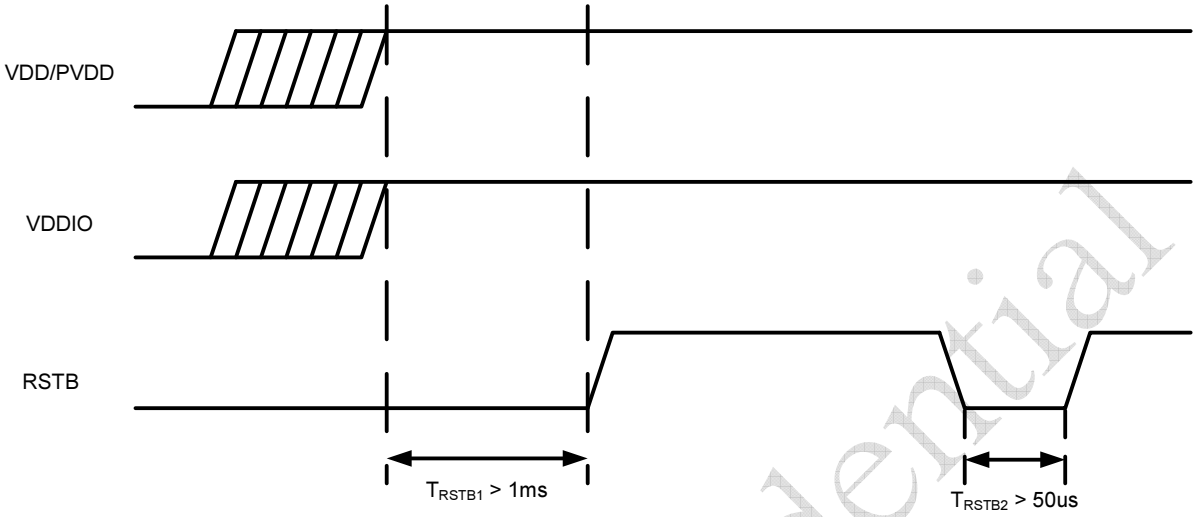
10.1 Power-On Sequence



10.2 Power-Off Sequence

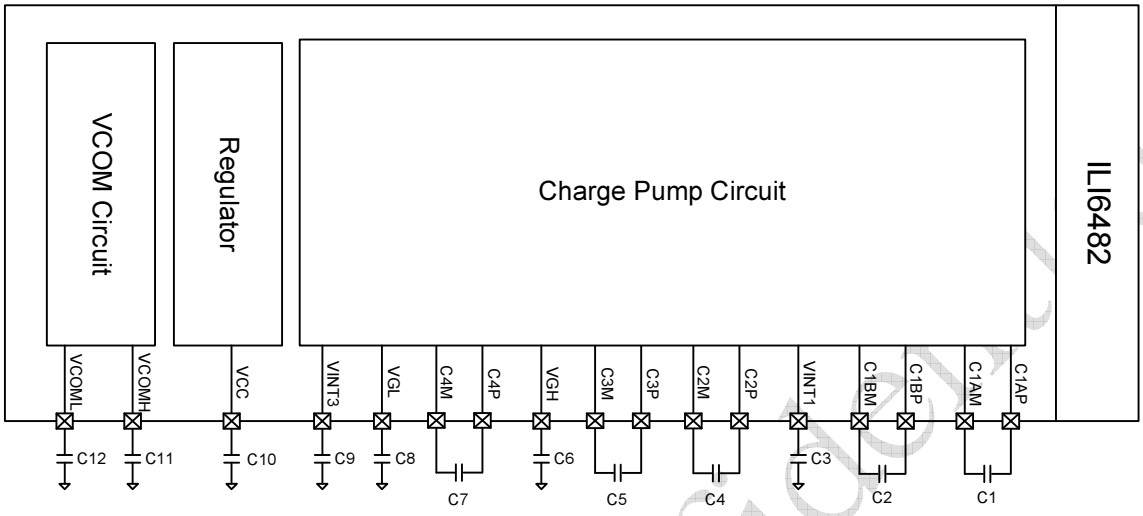


10.3 External Reset for Power-On Sequence



To prevent from abnormal reset condition, please follow T_{RSTB1} and T_{RSTB2} timing specification.

10.4 Charge-Pump Circuit Connection



Component	Value	Voltage proof
C1	1µF	6.3V
C2	1µF	6.3V
C3	1µF	10V
C4	1µF	16V
C5	1µF	16V
C6	1µF	25V
C7	1µF	6.3V
C8	1µF	25V
C9	1µF	6.3V
C10	1µF	6.3V
C11	4.7µF	6.3V
C12	4.7µF	6.3V

11. Input Data and Output Voltage

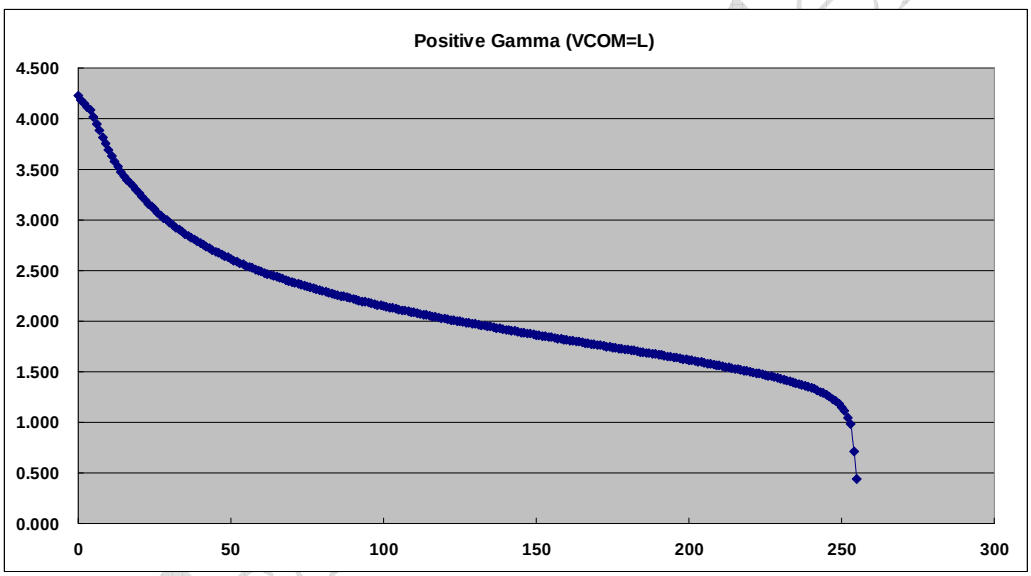
The sepuence for source data delivery could be controlled by “SHLR.”

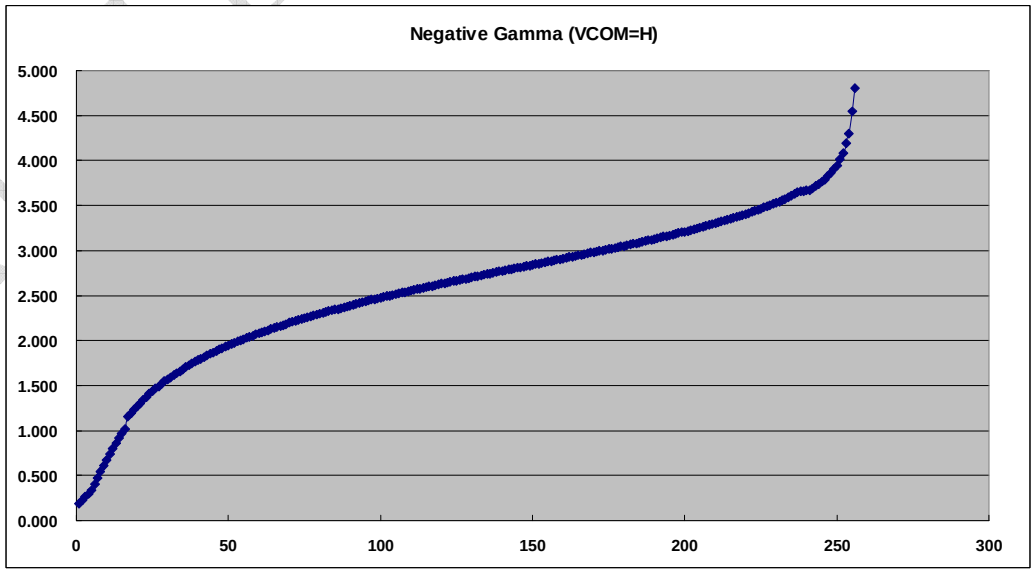
Output	S1	S2	S3	…	S718	S719	S720
SHLR=“1”	1st Data	→					Last Data
SHLR=“0”	Last Data	←					1st Data

The sepuence for gate scan could be controlled by “UPDN.”

Output	G1	G2	G3	…	G542	G543	G544
UPDN=“1”	1st Data	→					Last Data
UPDN=“0”	Last Data	←					1st Data

The below figures show the positive and the negative Gamma curves corresponding to 256 gray scales. The values of Gamma voltages calculated by our resistor design are presented in the following pages.





Input Data and Output Voltage Reference Table

Vno.	Data	VCOMOUT=H	Vno.	Data	VCOMOUT=H	Vno	Data	VCOMOUT=L	Vno.	Data	VCOMOUT=L
	00	0.185		80	2.694		00	4.225		80	1.980
	01	0.225		81	2.702		01	4.188		81	1.975
	02	0.265		82	2.709		02	4.151		82	1.970
	03	0.298		83	2.716		03	4.118		83	1.964
	04	0.331		84	2.723		04	4.086		84	1.959
	05	0.404		85	2.731		05	4.018		85	1.954
	06	0.477		86	2.738		06	3.951		86	1.949
	07	0.543		87	2.745		07	3.885		87	1.943
	08	0.609		88	2.753		08	3.820		88	1.938
	09	0.675		89	2.760		09	3.755		89	1.933
	0A	0.742		8A	2.767		0A	3.689		8A	1.927
	0B	0.801		8B	2.774		0B	3.635		8B	1.922
	0C	0.861		8C	2.782		0C	3.581		8C	1.917
	0D	0.914		8D	2.788		0D	3.526		8D	1.911
	0E	0.967		8E	2.795		0E	3.472		8E	1.906
	0F	1.016		8F	2.801		0F	3.430		8F	1.901
	10	1.153		90	2.808		10	3.398		90	1.895
	11	1.191		91	2.814		11	3.366		91	1.890
	12	1.229		92	2.821		12	3.334		92	1.884
	13	1.268		93	2.827		13	3.302		93	1.879
	14	1.306		94	2.833		14	3.266		94	1.874
	15	1.339		95	2.840		15	3.231		95	1.869
	16	1.373		96	2.847		16	3.196		96	1.864
	17	1.406		97	2.854		17	3.160		97	1.859
	18	1.439		98	2.861		18	3.131		98	1.854
	19	1.466		99	2.868		19	3.103		99	1.849
	1A	1.493		9A	2.875		1A	3.074		9A	1.844
	1B	1.520		9B	2.882		1B	3.045		9B	1.839
	1C	1.547		9C	2.889		1C	3.020		9C	1.834
	1D	1.570		9D	2.896		1D	2.996		9D	1.829
	1E	1.593		9E	2.903		1E	2.971		9E	1.824
	1F	1.615		9F	2.910		1F	2.947		9F	1.819
	20	1.638		A0	2.917		20	2.925		A0	1.814
	21	1.659		A1	2.924		21	2.903		A1	1.809
	22	1.681		A2	2.931		22	2.882		A2	1.804
	23	1.703		A3	2.938		23	2.860		A3	1.799
	24	1.725		A4	2.946		24	2.841		A4	1.794
	25	1.744		A5	2.953		25	2.823		A5	1.789
	26	1.762		A6	2.960		26	2.804		A6	1.784
	27	1.781		A7	2.967		27	2.786		A7	1.779
	28	1.799		A8	2.974		28	2.769		A8	1.774
	29	1.817		A9	2.981		29	2.752		A9	1.769
	2A	1.834		AA	2.988		2A	2.735		AA	1.764
	2B	1.851		AB	2.995		2B	2.718		AB	1.759
	2C	1.868		AC	3.002		2C	2.703		AC	1.754
	2D	1.884		AD	3.009		2D	2.687		AD	1.749
	2E	1.900		AE	3.016		2E	2.672		AE	1.744
	2F	1.916		AF	3.023		2F	2.657		AF	1.739
	30	1.932		B0	3.030		30	2.643		B0	1.734
	31	1.946		B1	3.037		31	2.629		B1	1.730
	32	1.961		B2	3.044		32	2.614		B2	1.726
	33	1.976		B3	3.051		33	2.600		B3	1.721
	34	1.990		B4	3.058		34	2.587		B4	1.716
	35	2.003		B5	3.066		35	2.574		B5	1.711
	36	2.017		B6	3.074		36	2.561		B6	1.706
	37	2.030		B7	3.082		37	2.548		B7	1.701
	38	2.043		B8	3.089		38	2.536		B8	1.696
	39	2.055		B9	3.097		39	2.524		B9	1.692
	3A	2.067		BA	3.105		3A	2.512		BA	1.687
	3B	2.079		BB	3.113		3B	2.500		BB	1.682
	3C	2.091		BC	3.121		3C	2.489		BC	1.677
	3D	2.103		BD	3.129		3D	2.478		BD	1.672
	3E	2.115		BE	3.137		3E	2.467		BE	1.667
	3F	2.127		BF	3.144		3F	2.456		BF	1.662

	40	2.139		C0	3.152
	41	2.150		C1	3.160
	42	2.161		C2	3.168
	43	2.173		C3	3.176
	44	2.184		C4	3.184
	45	2.194		C5	3.192
	46	2.205		C6	3.201
	47	2.216		C7	3.209
	48	2.226		C8	3.218
	49	2.237		C9	3.227
	4A	2.247		CA	3.236
	4B	2.258		CB	3.245
	4C	2.268		CC	3.254
	4D	2.278		CD	3.263
	4E	2.287		CE	3.272
	4F	2.296		CF	3.282
	50	2.305		D0	3.291
	51	2.315		D1	3.301
	52	2.324		D2	3.310
	53	2.333		D3	3.320
	54	2.342		D4	3.330
	55	2.352		D5	3.340
	56	2.361		D6	3.351
	57	2.370		D7	3.361
	58	2.379		D8	3.372
	59	2.389		D9	3.383
	5A	2.398		DA	3.394
	5B	2.407		DB	3.405
	5C	2.416		DC	3.416
	5D	2.425		DD	3.428
	5E	2.434		DE	3.440
	5F	2.442		DF	3.452
	60	2.451		E0	3.464
	61	2.459		E1	3.477
	62	2.467		E2	3.490
	63	2.475		E3	3.503
	64	2.482		E4	3.516
	65	2.490		E5	3.530
	66	2.498		E6	3.544
	67	2.506		E7	3.558
	68	2.514		E8	3.572
	69	2.522		E9	3.592
	6A	2.530		EA	3.611
	6B	2.538		EB	3.631
	6C	2.546		EC	3.650
	6D	2.554		ED	3.655
	6E	2.562		EE	3.660
	6F	2.570		EF	3.665
	70	2.578		F0	3.670
	71	2.585		F1	3.689
	72	2.592		F2	3.714
	73	2.600		F3	3.739
	74	2.607		F4	3.764
	75	2.614		F5	3.789
	76	2.621		F6	3.827
	77	2.629		F7	3.865
	78	2.636		F8	3.903
	79	2.643		F9	3.941
	7A	2.651		FA	4.011
	7B	2.658		FB	4.080
	7C	2.665		FC	4.190
	7D	2.672		FD	4.301
	7E	2.680		FE	4.550
	7F	2.687		FF	4.800

	40	2.446		C0	1.657
	41	2.436		C1	1.653
	42	2.427		C2	1.648
	43	2.417		C3	1.643
	44	2.407		C4	1.637
	45	2.397		C5	1.632
	46	2.387		C6	1.627
	47	2.377		C7	1.621
	48	2.369		C8	1.616
	49	2.360		C9	1.610
	4A	2.351		CA	1.605
	4B	2.342		CB	1.599
	4C	2.334		CC	1.594
	4D	2.325		CD	1.589
	4E	2.316		CE	1.583
	4F	2.307		CF	1.578
	50	2.299		D0	1.572
	51	2.290		D1	1.566
	52	2.281		D2	1.560
	53	2.272		D3	1.554
	54	2.265		D4	1.548
	55	2.257		D5	1.542
	56	2.249		D6	1.536
	57	2.241		D7	1.530
	58	2.234		D8	1.524
	59	2.226		D9	1.518
	5A	2.218		DA	1.512
	5B	2.211		DB	1.506
	5C	2.204		DC	1.499
	5D	2.196		DD	1.493
	5E	2.189		DE	1.486
	5F	2.182		DF	1.480
	60	2.175		E0	1.473
	61	2.168		E1	1.466
	62	2.161		E2	1.460
	63	2.154		E3	1.453
	64	2.147		E4	1.445
	65	2.140		E5	1.438
	66	2.134		E6	1.430
	67	2.127		E7	1.422
	68	2.121		E8	1.414
	69	2.115		E9	1.406
	6A	2.109		EA	1.398
	6B	2.103		EB	1.390
	6C	2.097		EC	1.380
	6D	2.090		ED	1.370
	6E	2.084		EE	1.360
	6F	2.077		EF	1.350
	70	2.071		F0	1.340
	71	2.066		F1	1.331
	72	2.060		F2	1.316
	73	2.054		F3	1.301
	74	2.048		F4	1.288
	75	2.042		F5	1.275
	76	2.036		F6	1.253
	77	2.030		F7	1.230
	78	2.025		F8	1.208
	79	2.019		F9	1.185
	7A	2.013		FA	1.148
	7B	2.007		FB	1.110
	7C	2.002		FC	1.045
	7D	1.996		FD	0.98
	7E	1.991		FE	0.71
	7F	1.986		FF	0.44

12. Wire Resistance for Each Pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply so that the designed values do not exceed those recommendations.

Pin Name	Wiring resistance value (ohm)	Pin Name	Wiring resistance value (ohm)
VDD	<10	DEN	<50
PVDD	<3	DR0~DR7	<50
GND	<10	DG0~DG7	<50
AGND	<10	DB0~DB7	<50
PGND	<3	CSB	<50
VDDIO	<10	SDA	<50
VPP_OTP	<10	SCL	<50
VCC	<10	STB	<1000
VINT1	<5	GRB	<1000
VINT3	<10	HVDSL	<1000
C1AP/M	<5	UPDN	<1000
C1BP/M	<5	SHLR	<1000
C2P/M	<10	PINCTL	<1000
C3P/M	<10	PSEL	<1000
C4P/M	<10	TB1	<1000
VCOM	<5	EXT_PWR	<1000
VCOMH	<10	CLKPOL	<1000
VCOML	<10	VSDPOL	<1000
VGH	<10	HSDPOL	<1000
VGL	<10	FPOL	<1000
PWM_OUT	<50	DSWP	<1000
HSD	<50	RBSWP	<1000
VSD	<50	LHL	<1000
DCLK	<50	TCSW0	<1000

13. DC Characteristic

13.1 Absolute Maximum Rating

Logic supply voltage, VDDIO	-0.5V to 5V
Analog supply voltage, VINT1	-0.3V to 7.0V
VGL	-16V to 0.3V
VGH~VGL	-0.3V to 35V
Operating Ambient Temperature, TA	-20°C to 85°C
Storage Temperature, TSTR	-55°C to 125°C

The device stressed above those lists under “Absolute Maximum Ratings” operation may cause a permanent damage. The functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Range

(GND = AGND = PGND = 0V and TA = -20°C to 85°C)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Supply Voltage	VDD	3.0	3.3	3.6	V	
Charge Pump Supply Voltage	PVDD	3.0	3.3	3.6	V	
Digital Interface Supple Voltage	VDDIO	1.8	-	VDD	V	
Digital Input Voltage	Din	0	-	VDDIO	V	
OTP Supply Voltage	VPP_OTP	7.0	7.5	8.0-	V	
VCOM AC Voltage	VCOMH - VCOML	2.92	-	6.2	V	

13.2 DC Electrical Characteristic

(VDDIO=1.8V to VDD, VDD=3.0V to 3.6V, GND=AGND=PGND=0V, and TA= -20°C to 85°C)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Block Circuit						
Low Level Input Voltage	Vil	GND	-	0.3xVDDIO	V	Digital input pins
High Level Input Voltage	Vih	0.7xVDDIO	-	VDDIO	V	Digital input pins
Input Leakage Current	Ii	-	-	±1	µA	Digital input pins
Pull-high/low Impedance	Rin	-	200k	-	ohm	Digital control input pins @ VDDIO=3.3V
High Level Output Voltage	Voh	VDDIO-0.4	-	-	V	Digital input pins @ Ioh=400µA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins @ Iol=-400µA
Digital Stand-by Current	Idst	-	TBD	TBD	µA	Outputs @ High-Z & all pins are set default
Digital Operating Current	Icc	-	TBD	-	mA	DCLK=9MHz & Fld=17.28kHz In 24-bit RGB mode & without loading
Analog Block Circuit						
GAMMA reference voltage	VGAMH	-	5	-	V	
Step-up Circuit 1 Output Voltage	VINT1	5.4	-	-	V	
VCOMH Output Level	VCOMH	2.46		5	V	By VCOMH[6:0] setting
VCOML Output Level	VCOML	-3.0		-0.46	V	By VCOML[6:0] setting; VCOML>VINT3
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V ~ 0.5V & VDDA-0.5 ~ VDDA-0.1
		-	±15	±20	mV	Vo=0.5V ~ VDDA-0.5V
Dynamic Range of Ouput	Vdr	0.1	-	VDDA-0.1	V	S1 to S720
Low-level Output Current of VCOM	IOLC	-	TBD	-	mA	VCOMH=4V, VCOML=-1V VCOM output=-1V vs. -0.1V
High-level Output Current of VCOM	IOHC	-	TBD	-	mA	VCOMH=4V, VCOML=-1V VCOM output=4V vs. 3.1V
Source Low-level Output Current	IOLS	TBD	-	-	µA	S1 to S720; VO=0.1V vs. 1V
Source High-level Output Current	IOHS	TBD	-	-	µA	S1 to S720; VO=4.9V vs. 4.0V
Gate Low-level Output Current	IOLG	TBD	-	-	µA	G1 to G544; VO=VGL vs. VGL+0.5V
Gate High-level Output Current	IOHG	TBD	-	-	µA	G1 to G544; VO=VGH vs. VGH-0.5V
Analog Stand-by Current	Iast	-	-	100	µA	STB= “L,” All functions are shutdown
Analog Operating Current	IDD	-	TBD	-	mA	DCLK=9MHz, Fld=17.28kHz (@ 24bit RGB mode), No load

14. AC Characteristics

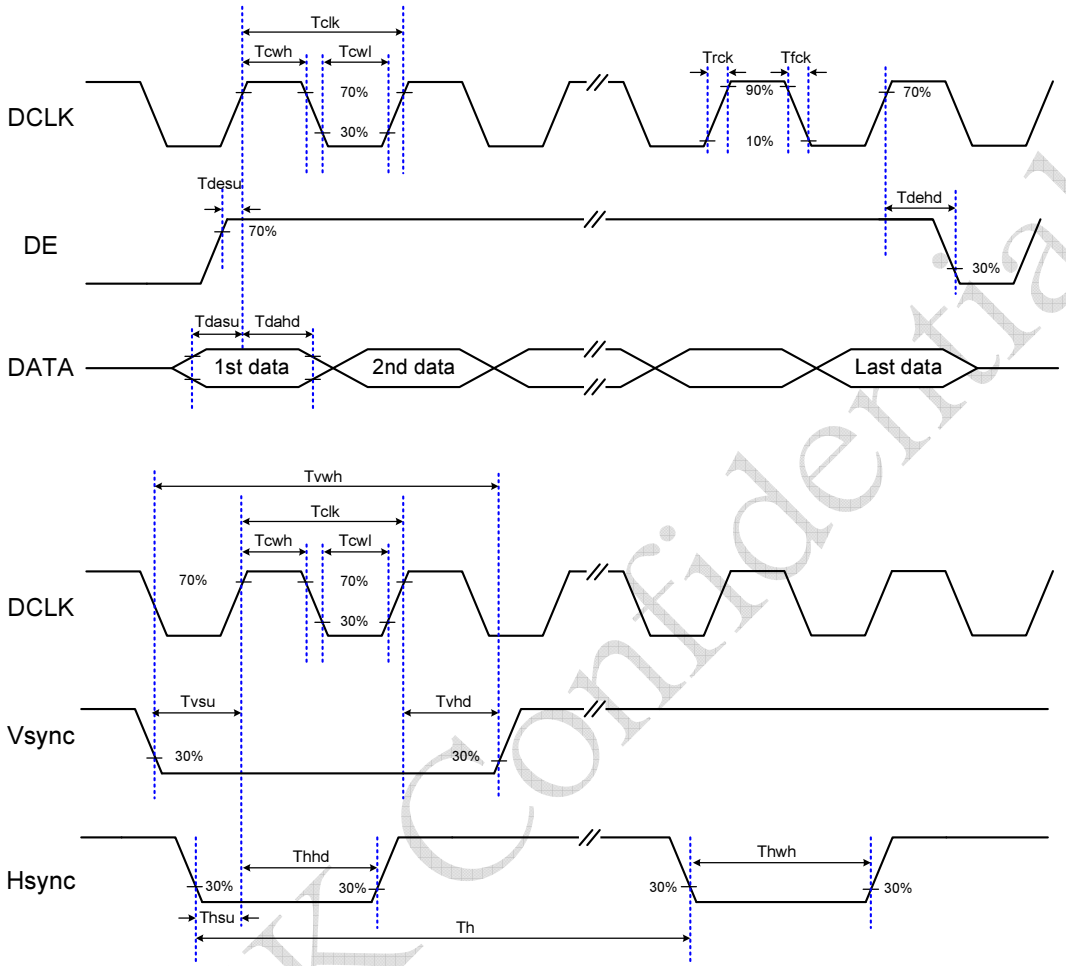
14.1 Input Signal Characteristics

AC Electrical Characteristics(VDDIO=1.8V to VDD, VDD=3.0V to 3.6V, GND=0V, and TA=-20°C to +85°C)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
System operation timing						
VDD power source slew time	TPOR	-	-	20	ms	From 0V to 0.99×VDD
GRB pulse width	tRSTW	10	50	-	μs	R=10kohm & C=1μF
Input output timing						
DCLK clock time	Tclk	33.3	-	-	ns	DCLK=30MHz
DCLK clock low period	Tcwl	40	-	60	%	
DCLK clock high period	Tcwh	40	-	60	%	
Clock rising time	Trck	9	-	-	ns	
Clock falling time	Tfck	9	-	-	ns	
HSD width	Thwh	1	-	-	DCLK	
HSD period time	Th	55	60	65	μs	
HSD setup time	Thsu	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
VSD width	Tvwh	1	-	-	Th	
VSD setup time	Tvsu	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
Data setup time	Tdasu	12	-	-	ns	
Data hold time	Tdahd	12	-	-	ns	
DE setup time	Tdesu	12	-	-	ns	
DE hold time	Tdehd	12	-	-	ns	
Source output setting time	Tsst	-	-	TBD	μs	10% to 90% CL=60pF & RL=2kohm
Gate output setting time	Tgst	-	-	TBD	ns	10% to 90% CL=60pF & RL=10kohm
VCOM output setting time	Tcst	-	-	TBD	μs	10% to 90% CL=40nF & RL=50ohm
Time from VSD to the data input of 1st line	Tvs	3	8	31	Th	HV mode By HDL[4:0] setting
3-wire serial communication AC timing						
Serial clock	Tsck	200	-	-	ns	For SCL pin
SCL pulse low period	Tckl	40	-	60	%	
SCL pulse low period	Tckh	40	-	60	%	
Serial data setup time	Tisu	50	-	-	ns	
Serial data hold time	Tihd	50	-	-	ns	
Serial clock high/low	Tssw	50	-	-	ns	
CSB to VSD	Tcv	1			μs	
CSB distinguish time	Tcd	400	-	-	ns	
CSB input setup time	Tcsu	50	-	-	ns	
CSB input hold time	Tchd	50	-	-	ns	

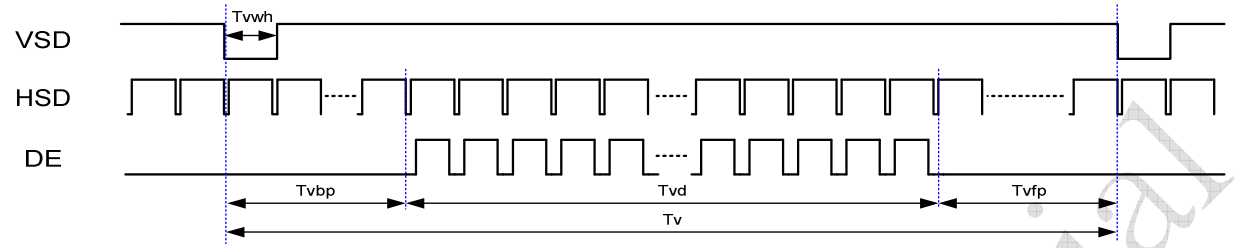
15. Timing Chart

15.1 Clock and Input Data Waveforms

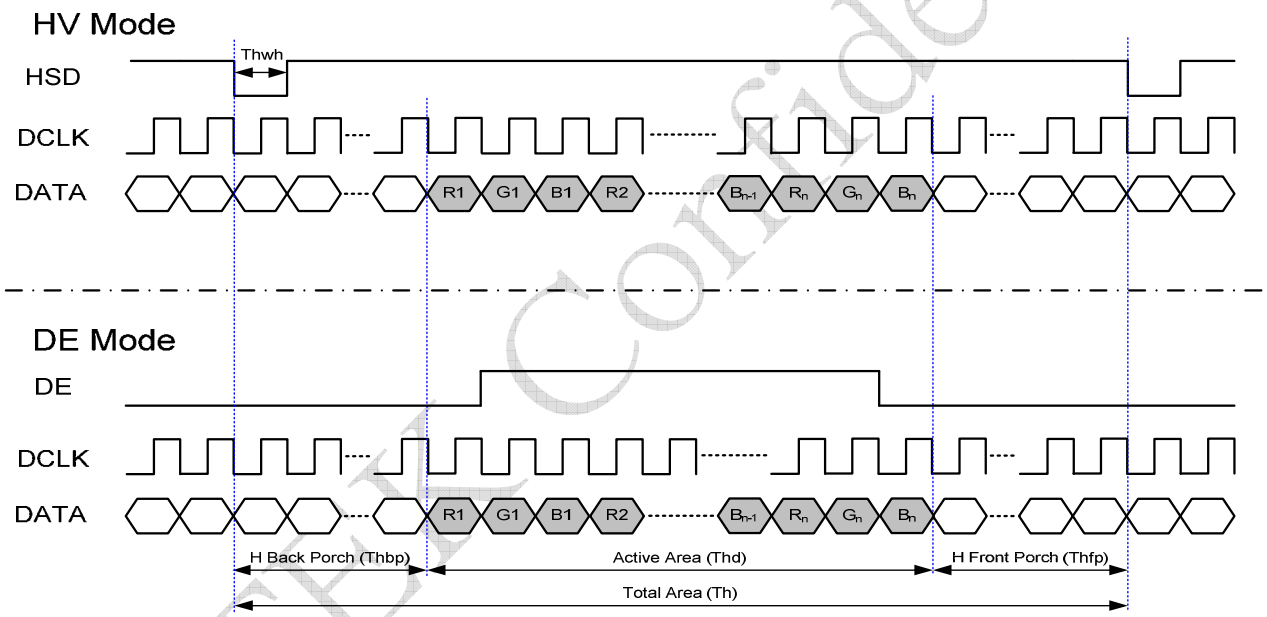


15.2 Data Input Format

Vertical Input Timing



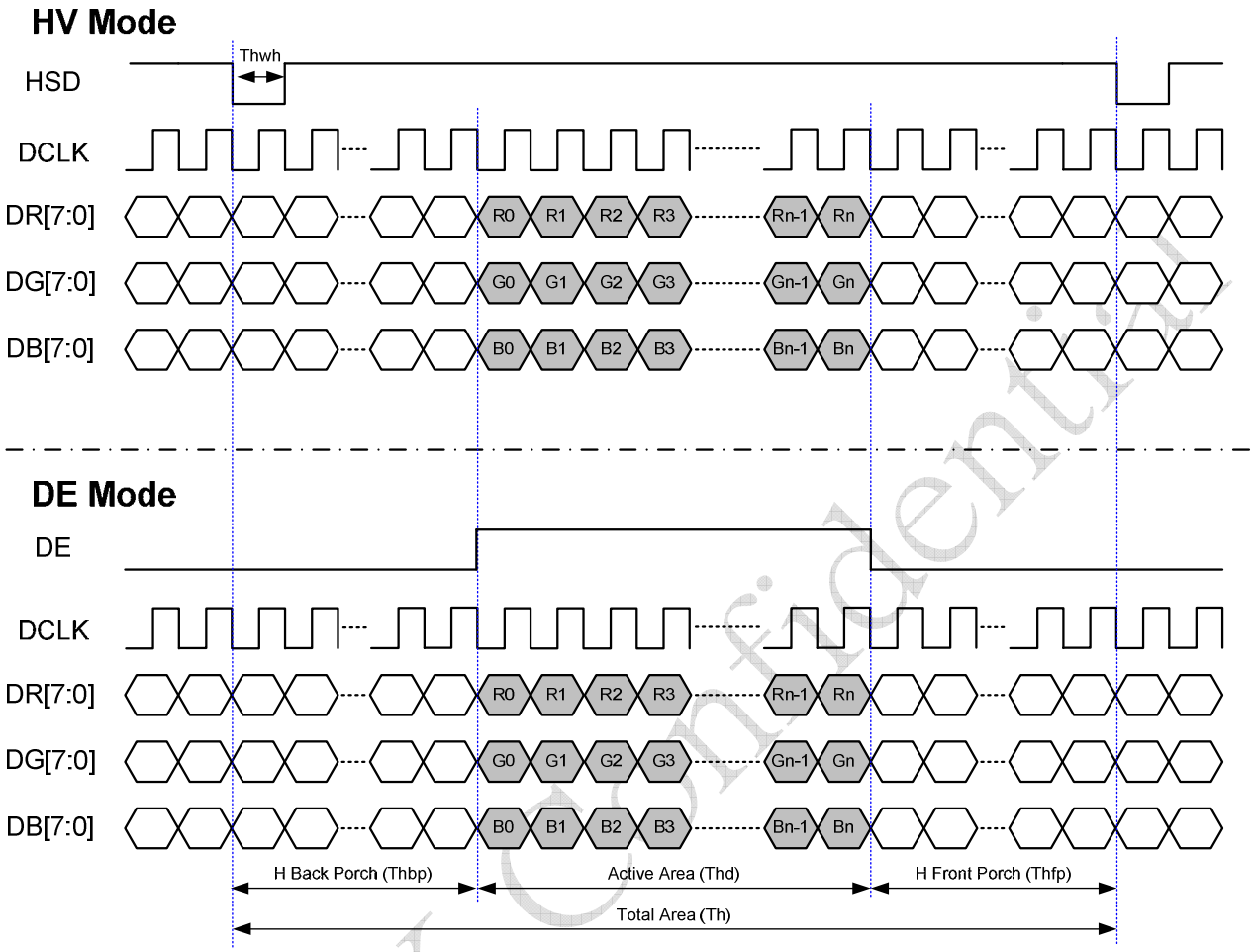
Serial 8bit RGB Mode Data Format



Serial RGB input timign table

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	-	27	-	MHz
VSD period time	Tv	277	288	400	H
VSD display area	Tvd		272		H
VSD back porch	Tvb	3	8	31	H
VSD front porch	Tvfp	2	8	97	H
HSD period time	Th	-	1728	-	DCLK
HSD display area	Thd		1440		DCLK
HSD back porch	Thbp	-	120	-	DCLK
HSD front porch	Thfp	-	168	-	DCLK

Parallel RGB mode data format

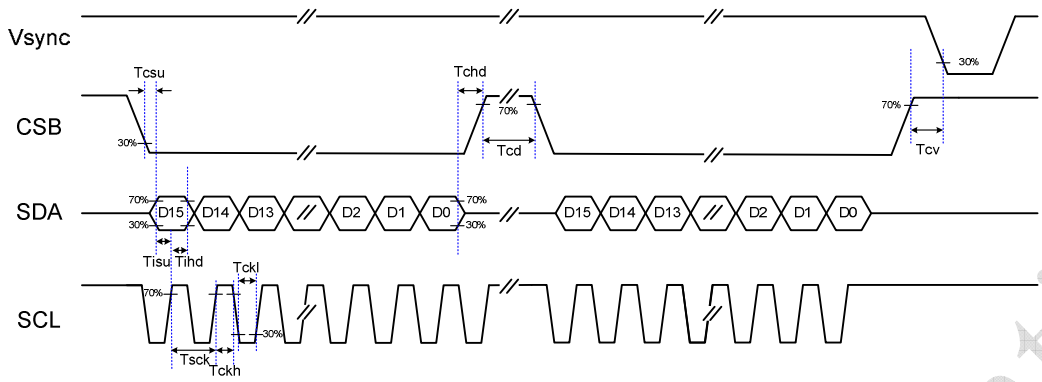


Parallel RGB input timign table

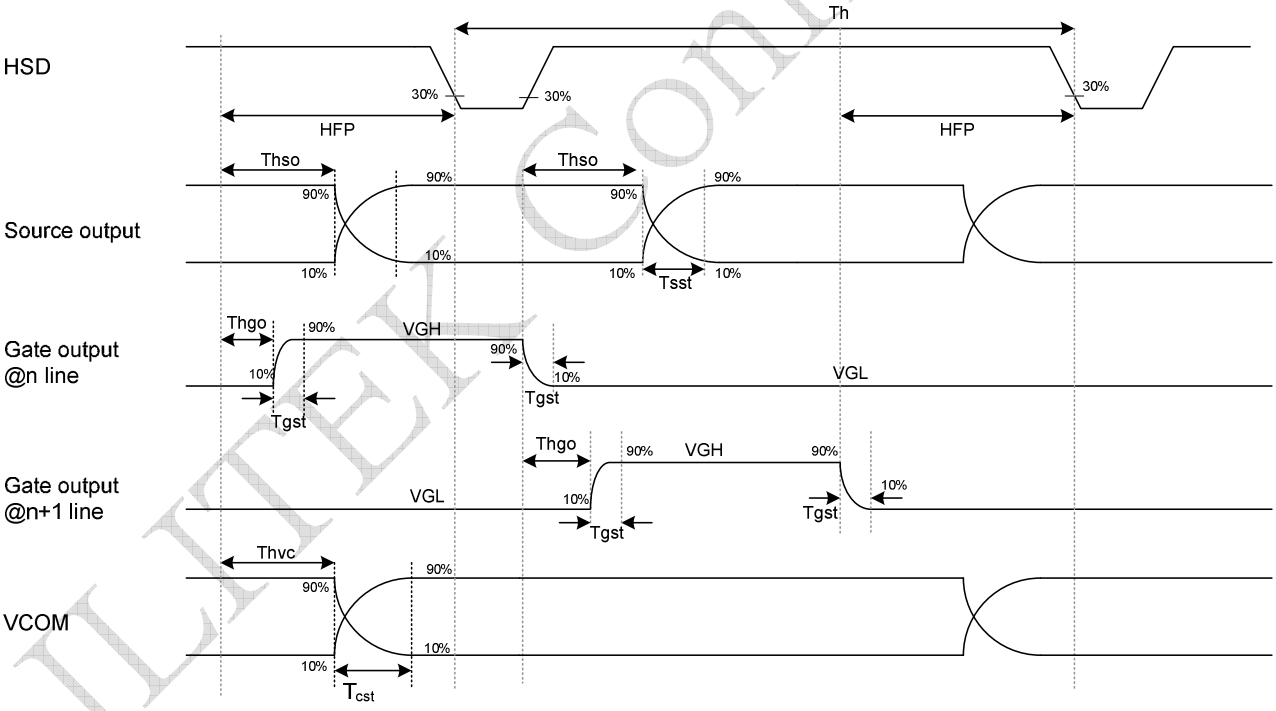
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	5	9	12	MHz
VSD period time	Tv	277	288	400	H
VSD display area	Tvd		272		H
VSD back porch	Tvb	3	8	31	H
VSD front porch	Tvfp	2	8	97	H
HSD period time	Th	520	525	800	DCLK
HSD display area	Thd		480		DCLK
HSD back porch	Thbp	36	40	255	DCLK
HSD front porch	Thfp	4	5	65	DCLK

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCLK frequency	Fclk	24	27	30	MHz	
DCLK cycle time	Tclk	83	110	200	ns	
DCLK pulse duty	Tcwh	40	50	60	%	
Time from HSD to source output	Thso	-	13	-	DCLK	
Time from HSD to gate output	Thgo	-	27	-	DCLK	
Time from HSD to gate output off	Thgz	-	3	-	DCLK	
Time from HSD to VCOM	Thvc	-	12	-	DCLK	

15.3 3-Wire Timing Diagram



15.4 Output Timing Diagram



16. Pad Location

No.	PAD name	X-axis	Y-axis
1	DUM	-9054.5	-240
2	DUM	-8963.5	-240
3	TP0	-8872.5	-240
4	TP1	-8781.5	-240
5	TP2	-8690.5	-240
6	TP3	-8599.5	-240
7	TP4	-8508.5	-240
8	TP5	-8417.5	-240
9	TP6	-8326.5	-240
10	TP7	-8235.5	-240
11	TP8	-8144.5	-240
12	TP9	-8053.5	-240
13	TP10	-7962.5	-240
14	DUMMY	-7871.5	-240
15	DUMMY	-7780.5	-240
16	DSWP	-7689.5	-240
17	RBSWP	-7598.5	-240
18	TB2	-7507.5	-240
19	LHL	-7416.5	-240
20	EXT_PWR	-7325.5	-240
21	FPOL	-7234.5	-240
22	VSDPOL	-7143.5	-240
23	HSDPOL	-7052.5	-240
24	CLKPOL	-6961.5	-240
25	TB0	-6870.5	-240
26	TB1	-6779.5	-240
27	TCSW0	-6688.5	-240
28	DUMMY	-6597.5	-240
29	VPP_OTP	-6506.5	-240
30	VPP_OTP	-6415.5	-240
31	VPP_OTP	-6324.5	-240
32	DUMMY	-6233.5	-240
33	SHIELDING	-6142.5	-240
34	COM1_L	-6051.5	-240
35	COM1_L	-5960.5	-240
36	SHIELDING	-5869.5	-240
37	VCOMH	-5778.5	-240
38	VCOMH	-5687.5	-240
39	VCOMH	-5596.5	-240
40	VCOMH	-5505.5	-240
41	VCOMH	-5414.5	-240
42	VCOML	-5323.5	-240
43	VCOML	-5232.5	-240
44	VCOML	-5141.5	-240
45	VCOML	-5050.5	-240
46	VCOML	-4959.5	-240
47	VCOML	-4868.5	-240
48	VCOM	-4777.5	-240
49	VCOM	-4686.5	-240
50	VCOM	-4595.5	-240

No.	PAD name	X-axis	Y-axis
51	VCOM	-4504.5	-240
52	VCOM	-4413.5	-240
53	VCOM	-4322.5	-240
54	VCOM	-4231.5	-240
55	VCOM	-4140.5	-240
56	VCOM	-4049.5	-240
57	VCOM	-3958.5	-240
58	GND	-3867.5	-240
59	GND	-3776.5	-240
60	GND	-3685.5	-240
61	GND	-3594.5	-240
62	VCC	-3503.5	-240
63	VCC	-3412.5	-240
64	VCC	-3321.5	-240
65	VDDIO	-3230.5	-240
66	VDDIO	-3139.5	-240
67	VDDIO	-3048.5	-240
68	VDD	-2957.5	-240
69	VDD	-2866.5	-240
70	VDD	-2775.5	-240
71	VDD	-2684.5	-240
72	VSD	-2593.5	-240
73	HSD	-2502.5	-240
74	DCLK	-2411.5	-240
75	DEN	-2320.5	-240
76	PSEL	-2229.5	-240
77	CSB	-2138.5	-240
78	SDA	-2047.5	-240
79	SCL	-1956.5	-240
80	STB	-1865.5	-240
81	GRB	-1774.5	-240
82	HVDSL	-1683.5	-240
83	UPDN	-1592.5	-240
84	SHLR	-1501.5	-240
85	PINCTL	-1410.5	-240
86	DUMMY	-1319.5	-240
87	SHIELDING	-1228.5	-240
88	DR0	-1137.5	-240
89	DR1	-1046.5	-240
90	DR2	-955.5	-240
91	DR3	-864.5	-240
92	DR4	-773.5	-240
93	DR5	-682.5	-240
94	DR6	-591.5	-240
95	DR7	-500.5	-240
96	DG0	-409.5	-240
97	DG1	-318.5	-240
98	DG2	-227.5	-240
99	DUMMY	-136.5	-240
100	DUMMY	-45.5	-240

No.	PAD name	X-axis	Y-axis
101	DUMMY	45.5	-240
102	DG3	136.5	-240
103	DG4	227.5	-240
104	DG5	318.5	-240
105	DG6	409.5	-240
106	DG7	500.5	-240
107	DB0	591.5	-240
108	DB1	682.5	-240
109	DB2	773.5	-240
110	DB3	864.5	-240
111	DB4	955.5	-240
112	DB5	1046.5	-240
113	DB6	1137.5	-240
114	DB7	1228.5	-240
115	DUMMY	1319.5	-240
116	SHIELDING	1410.5	-240
117	VSREF	1501.5	-240
118	AVDD	1592.5	-240
119	AVDD	1683.5	-240
120	AVDD	1774.5	-240
121	AVDD	1865.5	-240
122	AVDD	1956.5	-240
123	AVDD	2047.5	-240
124	AVDD	2138.5	-240
125	AVDD	2229.5	-240
126	AGND	2320.5	-240
127	AGND	2411.5	-240
128	AGND	2502.5	-240
129	AGND	2593.5	-240
130	VINT3	2684.5	-240
131	VINT3	2775.5	-240
132	VINT3	2866.5	-240
133	VINT3	2957.5	-240
134	VINT3	3048.5	-240
135	VINT3	3139.5	-240
136	C4M	3230.5	-240
137	C4M	3321.5	-240
138	C4M	3412.5	-240
139	C4M	3503.5	-240
140	C4P	3594.5	-240
141	C4P	3685.5	-240
142	C4P	3776.5	-240
143	C4P	3867.5	-240
144	VINT1	3958.5	-240
145	VINT1	4049.5	-240
146	VINT1	4140.5	-240
147	VINT1	4231.5	-240
148	PGND	4322.5	-240
149	PGND	4413.5	-240
150	PGND	4504.5	-240

No.	PAD name	X-axis	Y-axis
151	PGND	4595.5	-240
152	PGND	4686.5	-240
153	PGND	4777.5	-240
154	PGND	4868.5	-240
155	PGND	4959.5	-240
156	PGND	5050.5	-240
157	PGND	5141.5	-240
158	COM2_L	5232.5	-240
159	COM2_L	5323.5	-240
160	C1AP	5414.5	-240
161	C1AP	5505.5	-240
162	C1AP	5596.5	-240
163	C1AP	5687.5	-240
164	C1AM	5778.5	-240
165	C1AM	5869.5	-240
166	C1AM	5960.5	-240
167	C1AM	6051.5	-240
168	C1BP	6142.5	-240
169	C1BP	6233.5	-240
170	C1BP	6324.5	-240
171	C1BP	6415.5	-240
172	C1BM	6506.5	-240
173	C1BM	6597.5	-240
174	C1BM	6688.5	-240
175	C1BM	6779.5	-240
176	PVDD	6870.5	-240
177	PVDD	6961.5	-240
178	PVDD	7052.5	-240
179	PVDD	7143.5	-240
180	PVDD	7234.5	-240
181	PVDD	7325.5	-240
182	PVDD	7416.5	-240
183	PVDD	7507.5	-240
184	SHIELDING	7598.5	-240
185	C2P	7689.5	-240
186	C2P	7780.5	-240
187	C2M	7871.5	-240
188	C2M	7962.5	-240
189	VGH	8053.5	-240
190	VGH	8144.5	-240
191	VGH	8235.5	-240
192	C3P	8326.5	-240
193	C3P	8417.5	-240
194	C3M	8508.5	-240
195	C3M	8599.5	-240
196	VGL	8690.5	-240
197	VGL	8781.5	-240
198	VGL	8872.5	-240
199	DUM	8963.5	-240
200	DUM	9054.5	-240

No.	PAD name	X-axis	Y-axis
201	DUM	9226	211
202	G2	9212	79
203	G4	9198	211
204	G6	9184	79
205	G8	9170	211
206	G10	9156	79
207	G12	9142	211
208	G14	9128	79
209	G16	9114	211
210	G18	9100	79
211	G20	9086	211
212	G22	9072	79
213	G24	9058	211
214	G26	9044	79
215	G28	9030	211
216	G30	9016	79
217	G32	9002	211
218	G34	8988	79
219	G36	8974	211
220	G38	8960	79
221	G40	8946	211
222	G42	8932	79
223	G44	8918	211
224	G46	8904	79
225	G48	8890	211
226	G50	8876	79
227	G52	8862	211
228	G54	8848	79
229	G56	8834	211
230	G58	8820	79
231	G60	8806	211
232	G62	8792	79
233	G64	8778	211
234	G66	8764	79
235	G68	8750	211
236	G70	8736	79
237	G72	8722	211
238	G74	8708	79
239	G76	8694	211
240	G78	8680	79
241	G80	8666	211
242	G82	8652	79
243	G84	8638	211
244	G86	8624	79
245	G88	8610	211
246	G90	8596	79
247	G92	8582	211
248	G94	8568	79
249	G96	8554	211
250	G98	8540	79

No.	PAD name	X-axis	Y-axis
251	G100	8526	211
252	G102	8512	79
253	G104	8498	211
254	G106	8484	79
255	G108	8470	211
256	G110	8456	79
257	G112	8442	211
258	G114	8428	79
259	G116	8414	211
260	G118	8400	79
261	G120	8386	211
262	G122	8372	79
263	G124	8358	211
264	G126	8344	79
265	G128	8330	211
266	G130	8316	79
267	G132	8302	211
268	G134	8288	79
269	G136	8274	211
270	G138	8260	79
271	G140	8246	211
272	G142	8232	79
273	G144	8218	211
274	G146	8204	79
275	G148	8190	211
276	G150	8176	79
277	G152	8162	211
278	G154	8148	79
279	G156	8134	211
280	G158	8120	79
281	G160	8106	211
282	G162	8092	79
283	G164	8078	211
284	G166	8064	79
285	G168	8050	211
286	G170	8036	79
287	G172	8022	211
288	G174	8008	79
289	G176	7994	211
290	G178	7980	79
291	G180	7966	211
292	G182	7952	79
293	G184	7938	211
294	G186	7924	79
295	G188	7910	211
296	G190	7896	79
297	G192	7882	211
298	G194	7868	79
299	G196	7854	211
300	G198	7840	79

No.	PAD name	X-axis	Y-axis
301	G200	7826	211
302	G202	7812	79
303	G204	7798	211
304	G206	7784	79
305	G208	7770	211
306	G210	7756	79
307	G212	7742	211
308	G214	7728	79
309	G216	7714	211
310	G218	7700	79
311	G220	7686	211
312	G222	7672	79
313	G224	7658	211
314	G226	7644	79
315	G228	7630	211
316	G230	7616	79
317	G232	7602	211
318	G234	7588	79
319	G236	7574	211
320	G238	7560	79
321	G240	7546	211
322	G242	7532	79
323	G244	7518	211
324	G246	7504	79
325	G248	7490	211
326	G250	7476	79
327	G252	7462	211
328	G254	7448	79
329	G256	7434	211
330	G258	7420	79
331	G260	7406	211
332	G262	7392	79
333	G264	7378	211
334	G266	7364	79
335	G268	7350	211
336	G270	7336	79
337	G272	7322	211
338	G274	7308	79
339	G276	7294	211
340	G278	7280	79
341	G280	7266	211
342	G282	7252	79
343	G284	7238	211
344	G286	7224	79
345	G288	7210	211
346	G290	7196	79
347	G292	7182	211
348	G294	7168	79
349	G296	7154	211
350	G298	7140	79

No.	PAD name	X-axis	Y-axis
351	G300	7126	211
352	G302	7112	79
353	G304	7098	211
354	G306	7084	79
355	G308	7070	211
356	G310	7056	79
357	G312	7042	211
358	G314	7028	79
359	G316	7014	211
360	G318	7000	79
361	G320	6986	211
362	G322	6972	79
363	G324	6958	211
364	G326	6944	79
365	G328	6930	211
366	G330	6916	79
367	G332	6902	211
368	G334	6888	79
369	G336	6874	211
370	G338	6860	79
371	G340	6846	211
372	G342	6832	79
373	G344	6818	211
374	G346	6804	79
375	G348	6790	211
376	G350	6776	79
377	G352	6762	211
378	G354	6748	79
379	G356	6734	211
380	G358	6720	79
381	G360	6706	211
382	G362	6692	79
383	G364	6678	211
384	G366	6664	79
385	G368	6650	211
386	G370	6636	79
387	G372	6622	211
388	G374	6608	79
389	G376	6594	211
390	G378	6580	79
391	G380	6566	211
392	G382	6552	79
393	G384	6538	211
394	G386	6524	79
395	G388	6510	211
396	G390	6496	79
397	G392	6482	211
398	G394	6468	79
399	G396	6454	211
400	G398	6440	79

No.	PAD name	X-axis	Y-axis
401	G400	6426	211
402	G402	6412	79
403	G404	6398	211
404	G406	6384	79
405	G408	6370	211
406	G410	6356	79
407	G412	6342	211
408	G414	6328	79
409	G416	6314	211
410	G418	6300	79
411	G420	6286	211
412	G422	6272	79
413	G424	6258	211
414	G426	6244	79
415	G428	6230	211
416	G430	6216	79
417	G432	6202	211
418	G434	6188	79
419	G436	6174	211
420	G438	6160	79
421	G440	6146	211
422	G442	6132	79
423	G444	6118	211
424	G446	6104	79
425	G448	6090	211
426	G450	6076	79
427	G452	6062	211
428	G454	6048	79
429	G456	6034	211
430	G458	6020	79
431	G460	6006	211
432	G462	5992	79
433	G464	5978	211
434	G466	5964	79
435	G468	5950	211
436	G470	5936	79
437	G472	5922	211
438	G474	5908	79
439	G476	5894	211
440	G478	5880	79
441	G480	5866	211
442	G482	5852	79
443	G484	5838	211
444	G486	5824	79
445	G488	5810	211
446	G490	5796	79
447	G492	5782	211
448	G494	5768	79
449	G496	5754	211
450	G498	5740	79

No.	PAD name	X-axis	Y-axis
451	G500	5726	211
452	G502	5712	79
453	G504	5698	211
454	G506	5684	79
455	G508	5670	211
456	G510	5656	79
457	G512	5642	211
458	G514	5628	79
459	G516	5614	211
460	G518	5600	79
461	G520	5586	211
462	G522	5572	79
463	G524	5558	211
464	G526	5544	79
465	G528	5530	211
466	G530	5516	79
467	G532	5502	211
468	G534	5488	79
469	G536	5474	211
470	G538	5460	79
471	G540	5446	211
472	G542	5432	79
473	G544	5418	211
474	DUM	5404	79
475	DUM	5390	211
476	COM2_R	5376	79
477	COM2_R	5362	211
478	COM2_R	5348	79
479	COM2_R	5334	211
480	COM2_R	5320	79
481	COM2_R	5306	211
482	COM2_R	5292	79
483	COM2_R	5278	211
484	COM2_R	5264	79
485	COM2_R	5250	211
486	DUM	5236	79
487	DUM	5222	211
488	S1	5208	79
489	S2	5194	211
490	S3	5180	79
491	S4	5166	211
492	S5	5152	79
493	S6	5138	211
494	S7	5124	79
495	S8	5110	211
496	S9	5096	79
497	S10	5082	211
498	S11	5068	79
499	S12	5054	211
500	S13	5040	79

No.	PAD name	X-axis	Y-axis
501	S14	5026	211
502	S15	5012	79
503	S16	4998	211
504	S17	4984	79
505	S18	4970	211
506	S19	4956	79
507	S20	4942	211
508	S21	4928	79
509	S22	4914	211
510	S23	4900	79
511	S24	4886	211
512	S25	4872	79
513	S26	4858	211
514	S27	4844	79
515	S28	4830	211
516	S29	4816	79
517	S30	4802	211
518	S31	4788	79
519	S32	4774	211
520	S33	4760	79
521	S34	4746	211
522	S35	4732	79
523	S36	4718	211
524	S37	4704	79
525	S38	4690	211
526	S39	4676	79
527	S40	4662	211
528	S41	4648	79
529	S42	4634	211
530	S43	4620	79
531	S44	4606	211
532	S45	4592	79
533	S46	4578	211
534	S47	4564	79
535	S48	4550	211
536	S49	4536	79
537	S50	4522	211
538	S51	4508	79
539	S52	4494	211
540	S53	4480	79
541	S54	4466	211
542	S55	4452	79
543	S56	4438	211
544	S57	4424	79
545	S58	4410	211
546	S59	4396	79
547	S60	4382	211
548	S61	4368	79
549	S62	4354	211
550	S63	4340	79

No.	PAD name	X-axis	Y-axis
551	S64	4326	211
552	S65	4312	79
553	S66	4298	211
554	S67	4284	79
555	S68	4270	211
556	S69	4256	79
557	S70	4242	211
558	S71	4228	79
559	S72	4214	211
560	S73	4200	79
561	S74	4186	211
562	S75	4172	79
563	S76	4158	211
564	S77	4144	79
565	S78	4130	211
566	S79	4116	79
567	S80	4102	211
568	S81	4088	79
569	S82	4074	211
570	S83	4060	79
571	S84	4046	211
572	S85	4032	79
573	S86	4018	211
574	S87	4004	79
575	S88	3990	211
576	S89	3976	79
577	S90	3962	211
578	S91	3948	79
579	S92	3934	211
580	S93	3920	79
581	S94	3906	211
582	S95	3892	79
583	S96	3878	211
584	S97	3864	79
585	S98	3850	211
586	S99	3836	79
587	S100	3822	211
588	S101	3808	79
589	S102	3794	211
590	S103	3780	79
591	S104	3766	211
592	S105	3752	79
593	S106	3738	211
594	S107	3724	79
595	S108	3710	211
596	S109	3696	79
597	S110	3682	211
598	S111	3668	79
599	S112	3654	211
600	S113	3640	79

No.	PAD name	X-axis	Y-axis
601	S114	3626	211
602	S115	3612	79
603	S116	3598	211
604	S117	3584	79
605	S118	3570	211
606	S119	3556	79
607	S120	3542	211
608	S121	3528	79
609	S122	3514	211
610	S123	3500	79
611	S124	3486	211
612	S125	3472	79
613	S126	3458	211
614	S127	3444	79
615	S128	3430	211
616	S129	3416	79
617	S130	3402	211
618	S131	3388	79
619	S132	3374	211
620	S133	3360	79
621	S134	3346	211
622	S135	3332	79
623	S136	3318	211
624	S137	3304	79
625	S138	3290	211
626	S139	3276	79
627	S140	3262	211
628	S141	3248	79
629	S142	3234	211
630	S143	3220	79
631	S144	3206	211
632	S145	3192	79
633	S146	3178	211
634	S147	3164	79
635	S148	3150	211
636	S149	3136	79
637	S150	3122	211
638	S151	3108	79
639	S152	3094	211
640	S153	3080	79
641	S154	3066	211
642	S155	3052	79
643	S156	3038	211
644	S157	3024	79
645	S158	3010	211
646	S159	2996	79
647	S160	2982	211
648	S161	2968	79
649	S162	2954	211
650	S163	2940	79

No.	PAD name	X-axis	Y-axis
651	S164	2926	211
652	S165	2912	79
653	S166	2898	211
654	S167	2884	79
655	S168	2870	211
656	S169	2856	79
657	S170	2842	211
658	S171	2828	79
659	S172	2814	211
660	S173	2800	79
661	S174	2786	211
662	S175	2772	79
663	S176	2758	211
664	S177	2744	79
665	S178	2730	211
666	S179	2716	79
667	S180	2702	211
668	S181	2688	79
669	S182	2674	211
670	S183	2660	79
671	S184	2646	211
672	S185	2632	79
673	S186	2618	211
674	S187	2604	79
675	S188	2590	211
676	S189	2576	79
677	S190	2562	211
678	S191	2548	79
679	S192	2534	211
680	S193	2520	79
681	S194	2506	211
682	S195	2492	79
683	S196	2478	211
684	S197	2464	79
685	S198	2450	211
686	S199	2436	79
687	S200	2422	211
688	S201	2408	79
689	S202	2394	211
690	S203	2380	79
691	S204	2366	211
692	S205	2352	79
693	S206	2338	211
694	S207	2324	79
695	S208	2310	211
696	S209	2296	79
697	S210	2282	211
698	S211	2268	79
699	S212	2254	211
700	S213	2240	79

No.	PAD name	X-axis	Y-axis
701	S214	2226	211
702	S215	2212	79
703	S216	2198	211
704	S217	2184	79
705	S218	2170	211
706	S219	2156	79
707	S220	2142	211
708	S221	2128	79
709	S222	2114	211
710	S223	2100	79
711	S224	2086	211
712	S225	2072	79
713	S226	2058	211
714	S227	2044	79
715	S228	2030	211
716	S229	2016	79
717	S230	2002	211
718	S231	1988	79
719	S232	1974	211
720	S233	1960	79
721	S234	1946	211
722	S235	1932	79
723	S236	1918	211
724	S237	1904	79
725	S238	1890	211
726	S239	1876	79
727	S240	1862	211
728	S241	1848	79
729	S242	1834	211
730	S243	1820	79
731	S244	1806	211
732	S245	1792	79
733	S246	1778	211
734	S247	1764	79
735	S248	1750	211
736	S249	1736	79
737	S250	1722	211
738	S251	1708	79
739	S252	1694	211
740	S253	1680	79
741	S254	1666	211
742	S255	1652	79
743	S256	1638	211
744	S257	1624	79
745	S258	1610	211
746	S259	1596	79
747	S260	1582	211
748	S261	1568	79
749	S262	1554	211
750	S263	1540	79

No.	PAD name	X-axis	Y-axis
751	S264	1526	211
752	S265	1512	79
753	S266	1498	211
754	S267	1484	79
755	S268	1470	211
756	S269	1456	79
757	S270	1442	211
758	S271	1428	79
759	S272	1414	211
760	S273	1400	79
761	S274	1386	211
762	S275	1372	79
763	S276	1358	211
764	S277	1344	79
765	S278	1330	211
766	S279	1316	79
767	S280	1302	211
768	S281	1288	79
769	S282	1274	211
770	S283	1260	79
771	S284	1246	211
772	S285	1232	79
773	S286	1218	211
774	S287	1204	79
775	S288	1190	211
776	S289	1176	79
777	S290	1162	211
778	S291	1148	79
779	S292	1134	211
780	S293	1120	79
781	S294	1106	211
782	S295	1092	79
783	S296	1078	211
784	S297	1064	79
785	S298	1050	211
786	S299	1036	79
787	S300	1022	211
788	S301	1008	79
789	S302	994	211
790	S303	980	79
791	S304	966	211
792	S305	952	79
793	S306	938	211
794	S307	924	79
795	S308	910	211
796	S309	896	79
797	S310	882	211
798	S311	868	79
799	S312	854	211
800	S313	840	79

No.	PAD name	X-axis	Y-axis
801	S314	826	211
802	S315	812	79
803	S316	798	211
804	S317	784	79
805	S318	770	211
806	S319	756	79
807	S320	742	211
808	S321	728	79
809	S322	714	211
810	S323	700	79
811	S324	686	211
812	S325	672	79
813	S326	658	211
814	S327	644	79
815	S328	630	211
816	S329	616	79
817	S330	602	211
818	S331	588	79
819	S332	574	211
820	S333	560	79
821	S334	546	211
822	S335	532	79
823	S336	518	211
824	S337	504	79
825	S338	490	211
826	S339	476	79
827	S340	462	211
828	S341	448	79
829	S342	434	211
830	S343	420	79
831	S344	406	211
832	S345	392	79
833	S346	378	211
834	S347	364	79
835	S348	350	211
836	S349	336	79
837	S350	322	211
838	S351	308	79
839	S352	294	211
840	S353	280	79
841	S354	266	211
842	S355	252	79
843	S356	238	211
844	S357	224	79
845	S358	210	211
846	S359	196	79
847	S360	182	211
848	DUM	168	79
849	DUM	154	211
850	DCMP	140	79

No.	PAD name	X-axis	Y-axis
851	DCMP	126	211
852	DCMP	112	79
853	DCMP	98	211
854	DCMP	84	79
855	DCMP	70	211
856	DCMP	56	79
857	DCMP	42	211
858	DCMP	28	79
859	DCMP	14	211
860	DCMP	0	79
861	DCMP	-14	211
862	DCMP	-28	79
863	DCMP	-42	211
864	DCMP	-56	79
865	DCMP	-70	211
866	DCMP	-84	79
867	DCMP	-98	211
868	DCMP	-112	79
869	DCMP	-126	211
870	DCMP	-140	79
871	DUM	-154	211
872	DUM	-168	79
873	S361	-182	211
874	S362	-196	79
875	S363	-210	211
876	S364	-224	79
877	S365	-238	211
878	S366	-252	79
879	S367	-266	211
880	S368	-280	79
881	S369	-294	211
882	S370	-308	79
883	S371	-322	211
884	S372	-336	79
885	S373	-350	211
886	S374	-364	79
887	S375	-378	211
888	S376	-392	79
889	S377	-406	211
890	S378	-420	79
891	S379	-434	211
892	S380	-448	79
893	S381	-462	211
894	S382	-476	79
895	S383	-490	211
896	S384	-504	79
897	S385	-518	211
898	S386	-532	79
899	S387	-546	211
900	S388	-560	79

No.	PAD name	X-axis	Y-axis
901	S389	-574	211
902	S390	-588	79
903	S391	-602	211
904	S392	-616	79
905	S393	-630	211
906	S394	-644	79
907	S395	-658	211
908	S396	-672	79
909	S397	-686	211
910	S398	-700	79
911	S399	-714	211
912	S400	-728	79
913	S401	-742	211
914	S402	-756	79
915	S403	-770	211
916	S404	-784	79
917	S405	-798	211
918	S406	-812	79
919	S407	-826	211
920	S408	-840	79
921	S409	-854	211
922	S410	-868	79
923	S411	-882	211
924	S412	-896	79
925	S413	-910	211
926	S414	-924	79
927	S415	-938	211
928	S416	-952	79
929	S417	-966	211
930	S418	-980	79
931	S419	-994	211
932	S420	-1008	79
933	S421	-1022	211
934	S422	-1036	79
935	S423	-1050	211
936	S424	-1064	79
937	S425	-1078	211
938	S426	-1092	79
939	S427	-1106	211
940	S428	-1120	79
941	S429	-1134	211
942	S430	-1148	79
943	S431	-1162	211
944	S432	-1176	79
945	S433	-1190	211
946	S434	-1204	79
947	S435	-1218	211
948	S436	-1232	79
949	S437	-1246	211
950	S438	-1260	79

No.	PAD name	X-axis	Y-axis
951	S439	-1274	211
952	S440	-1288	79
953	S441	-1302	211
954	S442	-1316	79
955	S443	-1330	211
956	S444	-1344	79
957	S445	-1358	211
958	S446	-1372	79
959	S447	-1386	211
960	S448	-1400	79
961	S449	-1414	211
962	S450	-1428	79
963	S451	-1442	211
964	S452	-1456	79
965	S453	-1470	211
966	S454	-1484	79
967	S455	-1498	211
968	S456	-1512	79
969	S457	-1526	211
970	S458	-1540	79
971	S459	-1554	211
972	S460	-1568	79
973	S461	-1582	211
974	S462	-1596	79
975	S463	-1610	211
976	S464	-1624	79
977	S465	-1638	211
978	S466	-1652	79
979	S467	-1666	211
980	S468	-1680	79
981	S469	-1694	211
982	S470	-1708	79
983	S471	-1722	211
984	S472	-1736	79
985	S473	-1750	211
986	S474	-1764	79
987	S475	-1778	211
988	S476	-1792	79
989	S477	-1806	211
990	S478	-1820	79
991	S479	-1834	211
992	S480	-1848	79
993	S481	-1862	211
994	S482	-1876	79
995	S483	-1890	211
996	S484	-1904	79
997	S485	-1918	211
998	S486	-1932	79
999	S487	-1946	211
1000	S488	-1960	79

No.	PAD name	X-axis	Y-axis
1001	S489	-1974	211
1002	S490	-1988	79
1003	S491	-2002	211
1004	S492	-2016	79
1005	S493	-2030	211
1006	S494	-2044	79
1007	S495	-2058	211
1008	S496	-2072	79
1009	S497	-2086	211
1010	S498	-2100	79
1011	S499	-2114	211
1012	S500	-2128	79
1013	S501	-2142	211
1014	S502	-2156	79
1015	S503	-2170	211
1016	S504	-2184	79
1017	S505	-2198	211
1018	S506	-2212	79
1019	S507	-2226	211
1020	S508	-2240	79
1021	S509	-2254	211
1022	S510	-2268	79
1023	S511	-2282	211
1024	S512	-2296	79
1025	S513	-2310	211
1026	S514	-2324	79
1027	S515	-2338	211
1028	S516	-2352	79
1029	S517	-2366	211
1030	S518	-2380	79
1031	S519	-2394	211
1032	S520	-2408	79
1033	S521	-2422	211
1034	S522	-2436	79
1035	S523	-2450	211
1036	S524	-2464	79
1037	S525	-2478	211
1038	S526	-2492	79
1039	S527	-2506	211
1040	S528	-2520	79
1041	S529	-2534	211
1042	S530	-2548	79
1043	S531	-2562	211
1044	S532	-2576	79
1045	S533	-2590	211
1046	S534	-2604	79
1047	S535	-2618	211
1048	S536	-2632	79
1049	S537	-2646	211
1050	S538	-2660	79

No.	PAD name	X-axis	Y-axis
1051	S539	-2674	211
1052	S540	-2688	79
1053	S541	-2702	211
1054	S542	-2716	79
1055	S543	-2730	211
1056	S544	-2744	79
1057	S545	-2758	211
1058	S546	-2772	79
1059	S547	-2786	211
1060	S548	-2800	79
1061	S549	-2814	211
1062	S550	-2828	79
1063	S551	-2842	211
1064	S552	-2856	79
1065	S553	-2870	211
1066	S554	-2884	79
1067	S555	-2898	211
1068	S556	-2912	79
1069	S557	-2926	211
1070	S558	-2940	79
1071	S559	-2954	211
1072	S560	-2968	79
1073	S561	-2982	211
1074	S562	-2996	79
1075	S563	-3010	211
1076	S564	-3024	79
1077	S565	-3038	211
1078	S566	-3052	79
1079	S567	-3066	211
1080	S568	-3080	79
1081	S569	-3094	211
1082	S570	-3108	79
1083	S571	-3122	211
1084	S572	-3136	79
1085	S573	-3150	211
1086	S574	-3164	79
1087	S575	-3178	211
1088	S576	-3192	79
1089	S577	-3206	211
1090	S578	-3220	79
1091	S579	-3234	211
1092	S580	-3248	79
1093	S581	-3262	211
1094	S582	-3276	79
1095	S583	-3290	211
1096	S584	-3304	79
1097	S585	-3318	211
1098	S586	-3332	79
1099	S587	-3346	211
1100	S588	-3360	79

No.	PAD name	X-axis	Y-axis
1101	S589	-3374	211
1102	S590	-3388	79
1103	S591	-3402	211
1104	S592	-3416	79
1105	S593	-3430	211
1106	S594	-3444	79
1107	S595	-3458	211
1108	S596	-3472	79
1109	S597	-3486	211
1110	S598	-3500	79
1111	S599	-3514	211
1112	S600	-3528	79
1113	S601	-3542	211
1114	S602	-3556	79
1115	S603	-3570	211
1116	S604	-3584	79
1117	S605	-3598	211
1118	S606	-3612	79
1119	S607	-3626	211
1120	S608	-3640	79
1121	S609	-3654	211
1122	S610	-3668	79
1123	S611	-3682	211
1124	S612	-3696	79
1125	S613	-3710	211
1126	S614	-3724	79
1127	S615	-3738	211
1128	S616	-3752	79
1129	S617	-3766	211
1130	S618	-3780	79
1131	S619	-3794	211
1132	S620	-3808	79
1133	S621	-3822	211
1134	S622	-3836	79
1135	S623	-3850	211
1136	S624	-3864	79
1137	S625	-3878	211
1138	S626	-3892	79
1139	S627	-3906	211
1140	S628	-3920	79
1141	S629	-3934	211
1142	S630	-3948	79
1143	S631	-3962	211
1144	S632	-3976	79
1145	S633	-3990	211
1146	S634	-4004	79
1147	S635	-4018	211
1148	S636	-4032	79
1149	S637	-4046	211
1150	S638	-4060	79

No.	PAD name	X-axis	Y-axis
1151	S639	-4074	211
1152	S640	-4088	79
1153	S641	-4102	211
1154	S642	-4116	79
1155	S643	-4130	211
1156	S644	-4144	79
1157	S645	-4158	211
1158	S646	-4172	79
1159	S647	-4186	211
1160	S648	-4200	79
1161	S649	-4214	211
1162	S650	-4228	79
1163	S651	-4242	211
1164	S652	-4256	79
1165	S653	-4270	211
1166	S654	-4284	79
1167	S655	-4298	211
1168	S656	-4312	79
1169	S657	-4326	211
1170	S658	-4340	79
1171	S659	-4354	211
1172	S660	-4368	79
1173	S661	-4382	211
1174	S662	-4396	79
1175	S663	-4410	211
1176	S664	-4424	79
1177	S665	-4438	211
1178	S666	-4452	79
1179	S667	-4466	211
1180	S668	-4480	79
1181	S669	-4494	211
1182	S670	-4508	79
1183	S671	-4522	211
1184	S672	-4536	79
1185	S673	-4550	211
1186	S674	-4564	79
1187	S675	-4578	211
1188	S676	-4592	79
1189	S677	-4606	211
1190	S678	-4620	79
1191	S679	-4634	211
1192	S680	-4648	79
1193	S681	-4662	211
1194	S682	-4676	79
1195	S683	-4690	211
1196	S684	-4704	79
1197	S685	-4718	211
1198	S686	-4732	79
1199	S687	-4746	211
1200	S688	-4760	79

No.	PAD name	X-axis	Y-axis
1201	S689	-4774	211
1202	S690	-4788	79
1203	S691	-4802	211
1204	S692	-4816	79
1205	S693	-4830	211
1206	S694	-4844	79
1207	S695	-4858	211
1208	S696	-4872	79
1209	S697	-4886	211
1210	S698	-4900	79
1211	S699	-4914	211
1212	S700	-4928	79
1213	S701	-4942	211
1214	S702	-4956	79
1215	S703	-4970	211
1216	S704	-4984	79
1217	S705	-4998	211
1218	S706	-5012	79
1219	S707	-5026	211
1220	S708	-5040	79
1221	S709	-5054	211
1222	S710	-5068	79
1223	S711	-5082	211
1224	S712	-5096	79
1225	S713	-5110	211
1226	S714	-5124	79
1227	S715	-5138	211
1228	S716	-5152	79
1229	S717	-5166	211
1230	S718	-5180	79
1231	S719	-5194	211
1232	S720	-5208	79
1233	DUM	-5222	211
1234	DUM	-5236	79
1235	COM1_R	-5250	211
1236	COM1_R	-5264	79
1237	COM1_R	-5278	211
1238	COM1_R	-5292	79
1239	COM1_R	-5306	211
1240	COM1_R	-5320	79
1241	COM1_R	-5334	211
1242	COM1_R	-5348	79
1243	COM1_R	-5362	211
1244	COM1_R	-5376	79
1245	DUM	-5390	211
1246	DUM	-5404	79
1247	G543	-5418	211
1248	G541	-5432	79
1249	G539	-5446	211
1250	G537	-5460	79

No.	PAD name	X-axis	Y-axis
1251	G535	-5474	211
1252	G533	-5488	79
1253	G531	-5502	211
1254	G529	-5516	79
1255	G527	-5530	211
1256	G525	-5544	79
1257	G523	-5558	211
1258	G521	-5572	79
1259	G519	-5586	211
1260	G517	-5600	79
1261	G515	-5614	211
1262	G513	-5628	79
1263	G511	-5642	211
1264	G509	-5656	79
1265	G507	-5670	211
1266	G505	-5684	79
1267	G503	-5698	211
1268	G501	-5712	79
1269	G499	-5726	211
1270	G497	-5740	79
1271	G495	-5754	211
1272	G493	-5768	79
1273	G491	-5782	211
1274	G489	-5796	79
1275	G487	-5810	211
1276	G485	-5824	79
1277	G483	-5838	211
1278	G481	-5852	79
1279	G479	-5866	211
1280	G477	-5880	79
1281	G475	-5894	211
1282	G473	-5908	79
1283	G471	-5922	211
1284	G469	-5936	79
1285	G467	-5950	211
1286	G465	-5964	79
1287	G463	-5978	211
1288	G461	-5992	79
1289	G459	-6006	211
1290	G457	-6020	79
1291	G455	-6034	211
1292	G453	-6048	79
1293	G451	-6062	211
1294	G449	-6076	79
1295	G447	-6090	211
1296	G445	-6104	79
1297	G443	-6118	211
1298	G441	-6132	79
1299	G439	-6146	211
1300	G437	-6160	79

No.	PAD name	X-axis	Y-axis
1301	G435	-6174	211
1302	G433	-6188	79
1303	G431	-6202	211
1304	G429	-6216	79
1305	G427	-6230	211
1306	G425	-6244	79
1307	G423	-6258	211
1308	G421	-6272	79
1309	G419	-6286	211
1310	G417	-6300	79
1311	G415	-6314	211
1312	G413	-6328	79
1313	G411	-6342	211
1314	G409	-6356	79
1315	G407	-6370	211
1316	G405	-6384	79
1317	G403	-6398	211
1318	G401	-6412	79
1319	G399	-6426	211
1320	G397	-6440	79
1321	G395	-6454	211
1322	G393	-6468	79
1323	G391	-6482	211
1324	G389	-6496	79
1325	G387	-6510	211
1326	G385	-6524	79
1327	G383	-6538	211
1328	G381	-6552	79
1329	G379	-6566	211
1330	G377	-6580	79
1331	G375	-6594	211
1332	G373	-6608	79
1333	G371	-6622	211
1334	G369	-6636	79
1335	G367	-6650	211
1336	G365	-6664	79
1337	G363	-6678	211
1338	G361	-6692	79
1339	G359	-6706	211
1340	G357	-6720	79
1341	G355	-6734	211
1342	G353	-6748	79
1343	G351	-6762	211
1344	G349	-6776	79
1345	G347	-6790	211
1346	G345	-6804	79
1347	G343	-6818	211
1348	G341	-6832	79
1349	G339	-6846	211
1350	G337	-6860	79

No.	PAD name	X-axis	Y-axis
1351	G335	-6874	211
1352	G333	-6888	79
1353	G331	-6902	211
1354	G329	-6916	79
1355	G327	-6930	211
1356	G325	-6944	79
1357	G323	-6958	211
1358	G321	-6972	79
1359	G319	-6986	211
1360	G317	-7000	79
1361	G315	-7014	211
1362	G313	-7028	79
1363	G311	-7042	211
1364	G309	-7056	79
1365	G307	-7070	211
1366	G305	-7084	79
1367	G303	-7098	211
1368	G301	-7112	79
1369	G299	-7126	211
1370	G297	-7140	79
1371	G295	-7154	211
1372	G293	-7168	79
1373	G291	-7182	211
1374	G289	-7196	79
1375	G287	-7210	211
1376	G285	-7224	79
1377	G283	-7238	211
1378	G281	-7252	79
1379	G279	-7266	211
1380	G277	-7280	79
1381	G275	-7294	211
1382	G273	-7308	79
1383	G271	-7322	211
1384	G269	-7336	79
1385	G267	-7350	211
1386	G265	-7364	79
1387	G263	-7378	211
1388	G261	-7392	79
1389	G259	-7406	211
1390	G257	-7420	79
1391	G255	-7434	211
1392	G253	-7448	79
1393	G251	-7462	211
1394	G249	-7476	79
1395	G247	-7490	211
1396	G245	-7504	79
1397	G243	-7518	211
1398	G241	-7532	79
1399	G239	-7546	211
1400	G237	-7560	79

No.	PAD name	X-axis	Y-axis
1401	G235	-7574	211
1402	G233	-7588	79
1403	G231	-7602	211
1404	G229	-7616	79
1405	G227	-7630	211
1406	G225	-7644	79
1407	G223	-7658	211
1408	G221	-7672	79
1409	G219	-7686	211
1410	G217	-7700	79
1411	G215	-7714	211
1412	G213	-7728	79
1413	G211	-7742	211
1414	G209	-7756	79
1415	G207	-7770	211
1416	G205	-7784	79
1417	G203	-7798	211
1418	G201	-7812	79
1419	G199	-7826	211
1420	G197	-7840	79
1421	G195	-7854	211
1422	G193	-7868	79
1423	G191	-7882	211
1424	G189	-7896	79
1425	G187	-7910	211
1426	G185	-7924	79
1427	G183	-7938	211
1428	G181	-7952	79
1429	G179	-7966	211
1430	G177	-7980	79
1431	G175	-7994	211
1432	G173	-8008	79
1433	G171	-8022	211
1434	G169	-8036	79
1435	G167	-8050	211
1436	G165	-8064	79
1437	G163	-8078	211
1438	G161	-8092	79
1439	G159	-8106	211
1440	G157	-8120	79
1441	G155	-8134	211
1442	G153	-8148	79
1443	G151	-8162	211
1444	G149	-8176	79
1445	G147	-8190	211
1446	G145	-8204	79
1447	G143	-8218	211
1448	G141	-8232	79
1449	G139	-8246	211
1450	G137	-8260	79

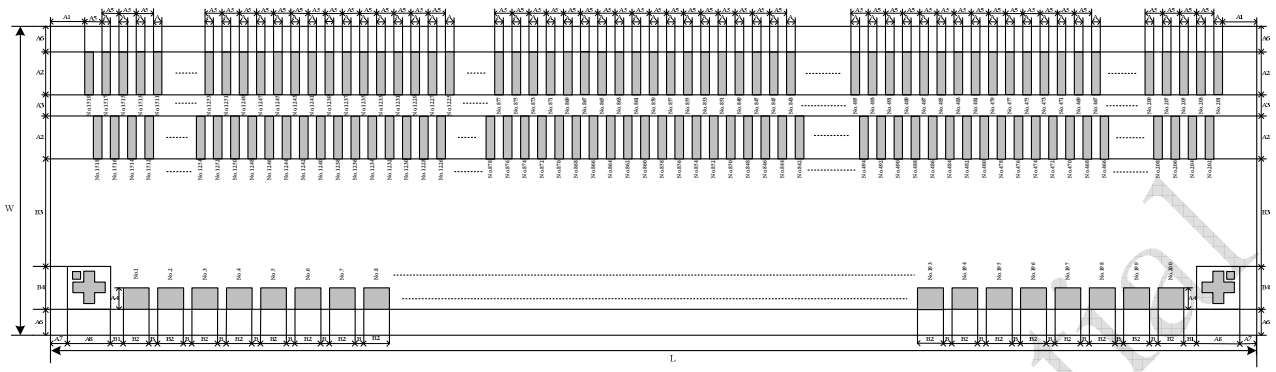
No.	PAD name	X-axis	Y-axis
1451	G135	-8274	211
1452	G133	-8288	79
1453	G131	-8302	211
1454	G129	-8316	79
1455	G127	-8330	211
1456	G125	-8344	79
1457	G123	-8358	211
1458	G121	-8372	79
1459	G119	-8386	211
1460	G117	-8400	79
1461	G115	-8414	211
1462	G113	-8428	79
1463	G111	-8442	211
1464	G109	-8456	79
1465	G107	-8470	211
1466	G105	-8484	79
1467	G103	-8498	211
1468	G101	-8512	79
1469	G99	-8526	211
1470	G97	-8540	79
1471	G95	-8554	211
1472	G93	-8568	79
1473	G91	-8582	211
1474	G89	-8596	79
1475	G87	-8610	211
1476	G85	-8624	79
1477	G83	-8638	211
1478	G81	-8652	79
1479	G79	-8666	211
1480	G77	-8680	79
1481	G75	-8694	211
1482	G73	-8708	79
1483	G71	-8722	211
1484	G69	-8736	79
1485	G67	-8750	211
1486	G65	-8764	79
1487	G63	-8778	211
1488	G61	-8792	79
1489	G59	-8806	211
1490	G57	-8820	79
1491	G55	-8834	211
1492	G53	-8848	79
1493	G51	-8862	211
1494	G49	-8876	79
1495	G47	-8890	211
1496	G45	-8904	79
1497	G43	-8918	211
1498	G41	-8932	79
1499	G39	-8946	211
1500	G37	-8960	79

No.	PAD name	X-axis	Y-axis
1501	G35	-8974	211
1502	G33	-8988	79
1503	G31	-9002	211
1504	G29	-9016	79
1505	G27	-9030	211
1506	G25	-9044	79
1507	G23	-9058	211
1508	G21	-9072	79
1509	G19	-9086	211
1510	G17	-9100	79
1511	G15	-9114	211
1512	G13	-9128	79
1513	G11	-9142	211
1514	G9	-9156	79
1515	G7	-9170	211
1516	G5	-9184	79
1517	G3	-9198	211
1518	G1	-9212	79
1519	DUM	-9226	211

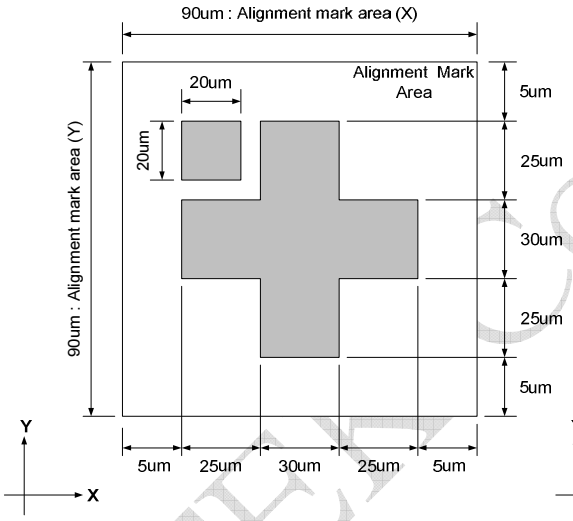
Alignment mark	X-axis	Y-axis
ALIGN_L	-9185	-205
ALIGN_R	9185	-205

Note: The coordinate of pads and alignment marks are after bonding process.

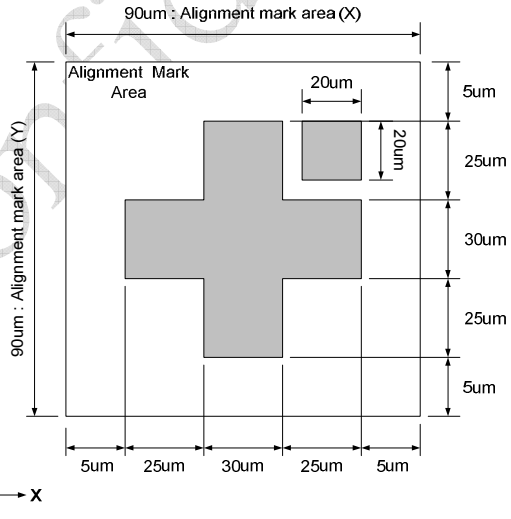
17. Bump Mask Information



Left Alignment Mark



Right Alignment Mark



Symbol	Dimension(um)
A	14
A1	72
A2	108
A3	24
A4	50
A5	28
A6	60
A7	75
A8	90

Symbol	Dimension(um)
B	30
B1	55
B2	61
B3	200
B4	90
W	650 (MAX)
L	18610 (MAX)
Bump Thickness	12

*Remark: Chip dimension includes scribe line.

18. Revision History

Version No.	Date	Page	Description
0.01	2011/09/08	All	New Creation