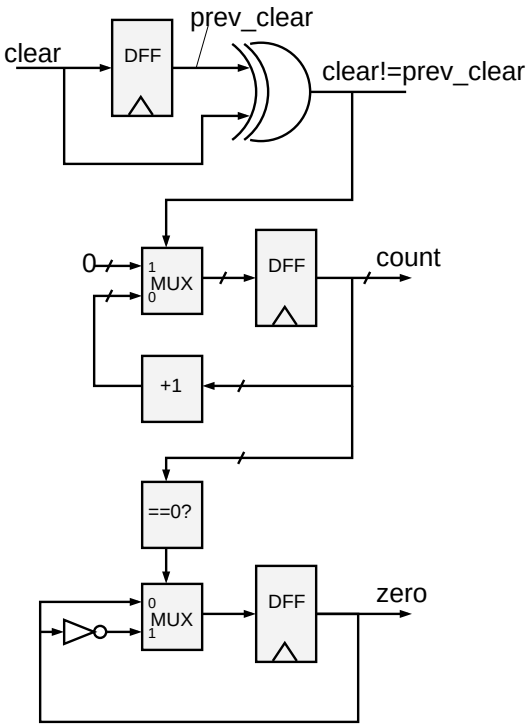
Example: Counter with NRZ control signals

Verilog description

```
module counter(clk,clear,zero);
  input clk,clear;
  output zero;

  reg [‘top:0] count;
  reg prev_clear;
  reg zero;

  always @(posedge clk) begin

    prev_clear <= clear;

    if (clear != prev_clear) count <= 0;
    else count <= count+1;

    if (count==0) zero <= ~zero;

  end
endmodule
```

Schematic diagram



(clock not shown)