Digital Electronics
Part II - Circuits

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Gates from Transistors

Introduction

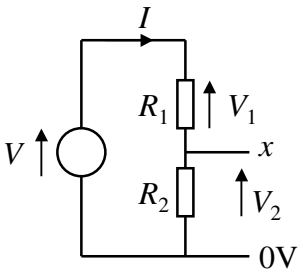
- Logic circuits are non-linear, consequently we will introduce a graphical technique for analysing such circuits
- The construction of an NMOS inverter from an n-channel field effect transistor (FET) is described
- CMOS logic is then introduced

Solving Non-linear circuits

- First of all we need to introduce Ohm's Law. For a linear component such as a resistor, this states that the voltage (V) across the device is proportional to the current (I) through it, i.e., $V = IR$
- We will apply this concept to a simple circuit consisting of 2 resistors in series connected across an ideal voltage source – known as a *potential divider*

Potential Divider

- What is the voltage at point x relative to the the 0V point?



$$V = V_1 + V_2$$

$$V_1 = IR_1 \qquad V_2 = IR_2$$

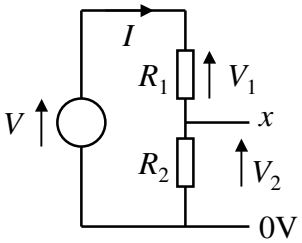
$$V = IR_1 + IR_2 = I(R_1 + R_2)$$

$$I = \frac{V}{(R_1 + R_2)}$$

$$V_x = V_2 = \frac{V}{(R_1 + R_2)} R_2 = V\left(\frac{R_2}{R_1 + R_2}\right)$$

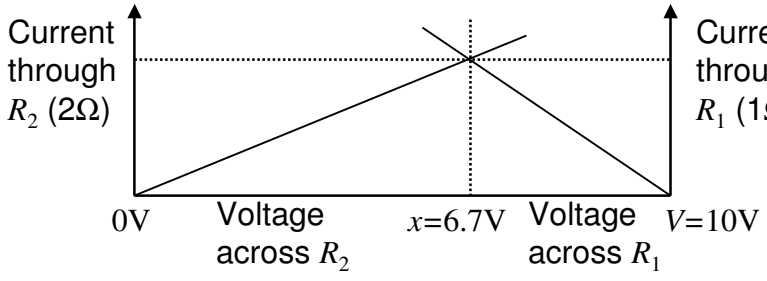
Potential Divider

- How can we do this graphically?



So if V = 10V, R_1 = 1Ω and R_2 = 2Ω

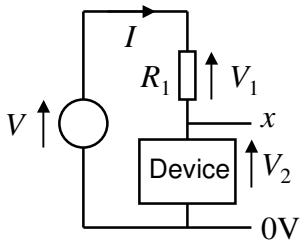
$$V_x = V\left(\frac{R_2}{R_1 + R_2}\right) = 10\left(\frac{2}{1+2}\right) = 6.7\text{V}$$



Graphical Approach

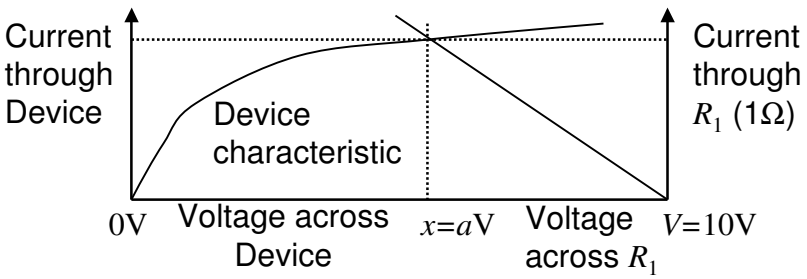
- Clearly approach works for a linear circuit.
- How could we apply this if we have a non-linear device, e.g., a transistor in place of R_2?
- What we do is substitute the V-I characteristic of the non-linear device in place of the linear characteristic (a straight line due to Ohm's Law) used previously for R_2

Graphical Approach



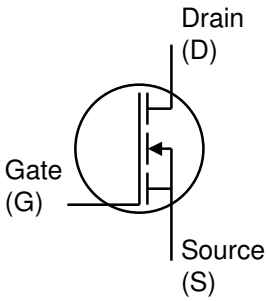
So if V = 10V and R_1 = 1Ω

The voltage at x is aV as shown in the graph



n-Channel MOSFET

- We will begin by assuming that the Device is a so called n-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

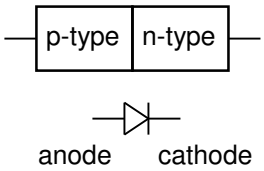


The current flow from D to S (I_{DS}) is controlled by the voltage applied between G and S (V_{GS})

We will be describing enhancement mode devices in which no current flows (I_{DS}=0, i.e., the transistor is Off) when V_{GS}=0V

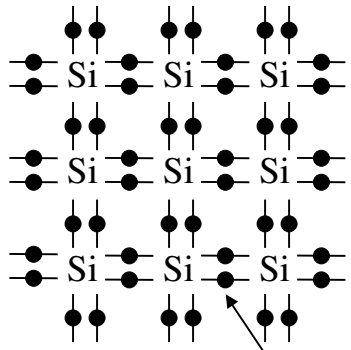
Diode

- To help us to understand the operation of the MOSFET, we will consider the operation of a more simple 2 terminal device known as a *diode*
- A diode is formed by the junction of so called n-type and p-type silicon (Si)



Semiconductors

- Silicon (Si, Group IV) is a poor conductor of electricity, i.e., a 'semiconductor'



Si crystalline lattice – poor conductor at low temperatures

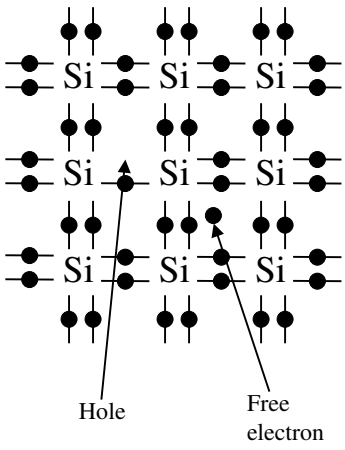
Si is *tetravalent*, i.e., it has 4 electrons in its *valance* band

Si crystals held together by *'covalent'* bonding

Recall that 8 valence electrons yield a stable state – each Si atom now appears to have 8 electrons, though in fact each atom only has a half share in them. Note this is a much more stable state than is the exclusive possession of 4 valence electrons

Semiconductors

- As temperature rises conductivity rises



As temperature rises, thermal vibration of the atoms causes bonds to break: electrons are free to wander around the crystal.

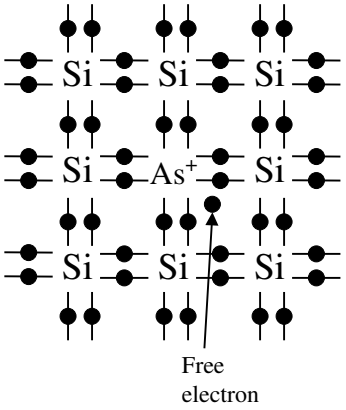
When an electron breaks free (i.e., moves into the *'conduction band'* it leaves behind a *'hole'* or absence of negative charge in the lattice

The hole can appear to move if it is filled by an electron from an adjacent atom

The availability of free electrons makes Si a conductor (a poor one)

n-type Si

- n-type silicon (Group IV) is doped with arsenic (Group V) that has an additional electron that is not involved in the bonds to the neighbouring Si atoms



The additional electron needs only a little energy to move into the conduction band.

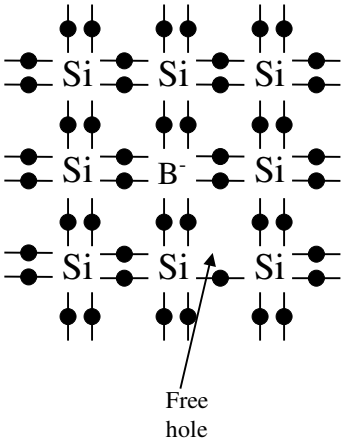
This electron is free to move around the lattice

Owing to its negative charge, the resulting semiconductor is known as *n-type*

Arsenic is known as a *donor* since it donates an electron

p-type Si

- p-type silicon (Group IV) is doped with boron (B, Group III)



The B atom has only 3 valence electrons, it accepts an extra electron from one of the adjacent Si atoms to complete its covalent bonds

This leaves a *hole* (i.e., absence of a valence electron) in the lattice

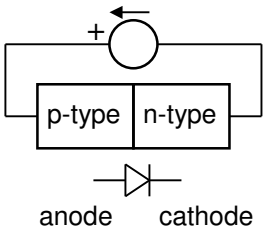
This hole is free to move in the lattice – actually it is the electrons that do the shifting, but the result is that the hole is shuffled from atom to atom.

The free hole has a positive charge, hence this semiconductor is *p-type*

B is known as an *acceptor*

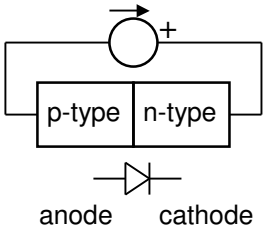
Diode

- When the voltage on the *anode* rises **above** the voltage on the *cathode*, the diode is said to be *forward biased*, and current flows through the diode from anode to cathode,
- i.e., electrons flow from n-type region into p-type region since they are attracted to the positive potential at the anode. Similarly holes flow from p to n region

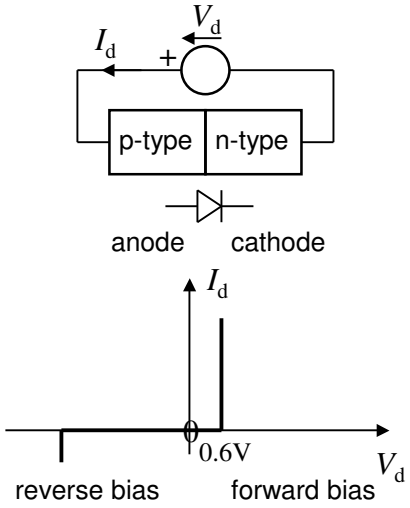


Diode

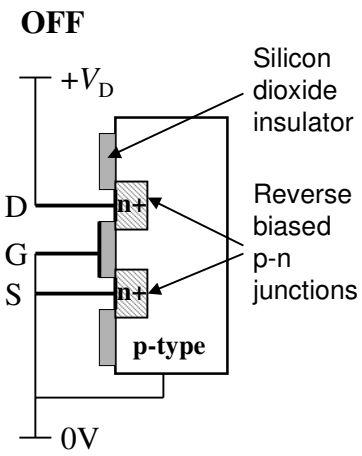
- When the voltage on the anode is **below** the voltage on the cathode, the diode is said to be *reverse biased*, and **no current** flows through the diode



Diode – Ideal Characteristic

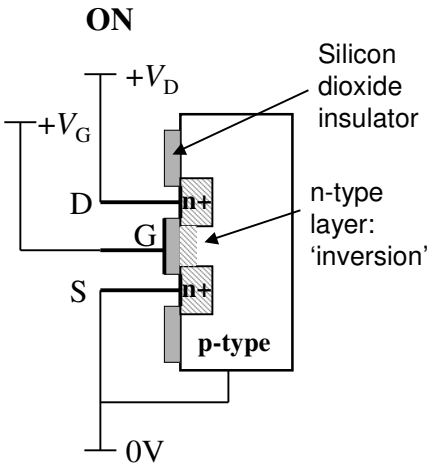


n-Channel MOSFET



Drain (and Source) diode reverse biased, so no path for current to flow from S to D, i.e., the transistor is **off**

n-Channel MOSFET



Consider the situation when the Gate (G) voltage (V_G) is raised to a positive voltage, say V_D

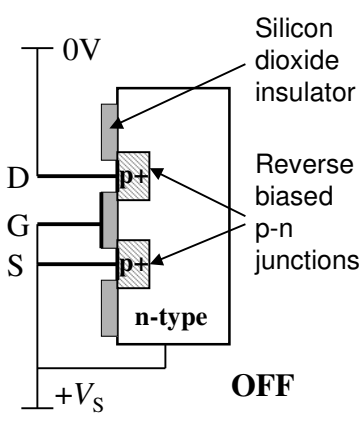
Electrons attracted to underside of the G, so this region is 'inverted' and becomes n-type. This region is known as the *channel*

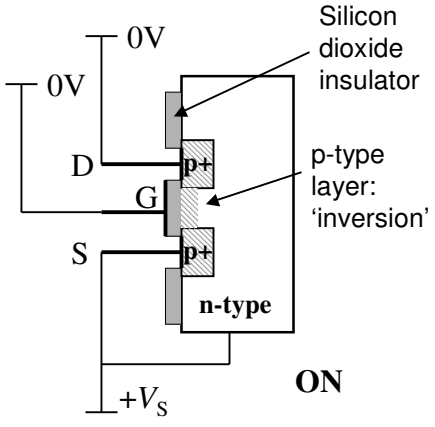
There is now a continuous path from n-type S to n-type D, so electrons can flow from S to D, i.e., the transistor is **on**

The G voltage (V_G) needed for this to occur is known as the *threshold voltage* (V_t). Typically 0.3 to 0.7 V.

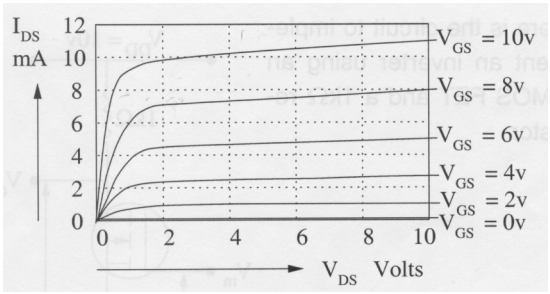
p-Channel MOSFET

- Two varieties, namely p and n channel
- p-channel have the opposite construction, i.e., n-type substrate and p-type S and D regions

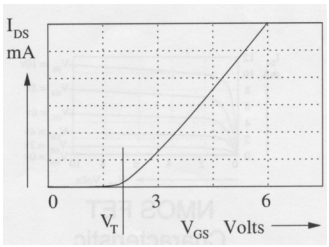




n-MOSFET Characteristics



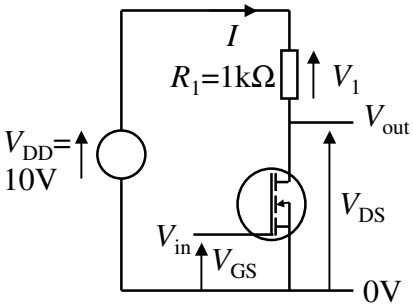
Plots V-I characteristics of the device for various Gate voltages (V_{GS})



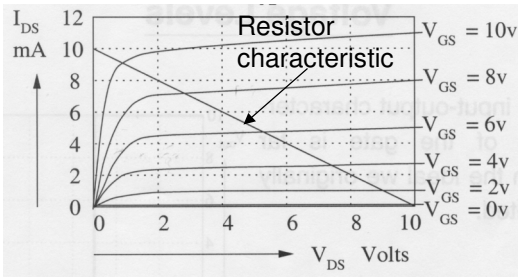
At a constant value of V_{DS} , we can also see that I_{DS} is a function of the Gate voltage, V_{GS}

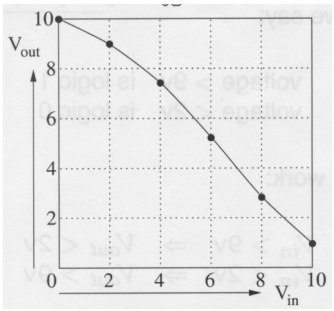
The transistor begins to conduct when the Gate voltage, V_{GS} , reaches the Threshold voltage: V_T

n-MOS Inverter



We can use the graphical approach to determine the relationship between V_{in} and V_{out}



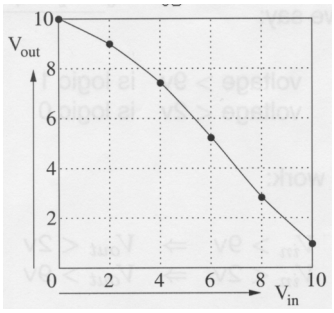


Note V_{in}=V_{GS} and V_{out}=V_{DS}

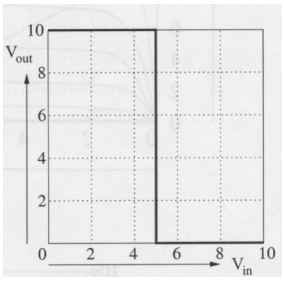
n-MOS Inverter

- Note it does not have the ‘ideal’ characteristic that we would like from an ‘inverter’ function

Actual



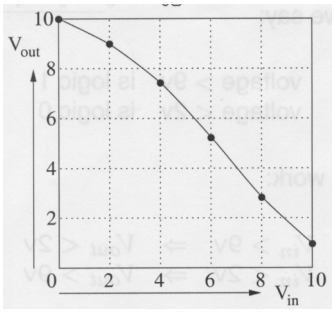
Ideal



However if we specify suitable voltage thresholds, we can achieve a ‘binary’ action.

n-MOS Inverter

Actual



So if we say:

voltage > 9V is logic 1

voltage < 2V is logic 0

The gate will work as follows:

V_{in} > 9V then V_{out} < 2V and if

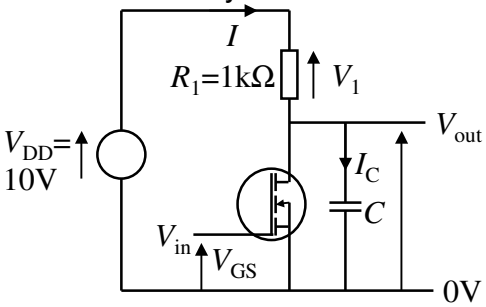
V_{in} < 2V then V_{out} > 9V

n-MOS Logic

- It is possible (and was done in the early days) to build other logic functions, e.g., NOR and NAND using n-MOS transistors
- However, n-MOS logic has fundamental problems:
  - Speed of operation
  - Power consumption

n-MOS Logic

- One of the main speed limitations is due to stray capacitance owing to the metal track used to connect gate inputs and outputs. This has a finite capacitance to ground
  - We modify the circuit model to include this capacitance



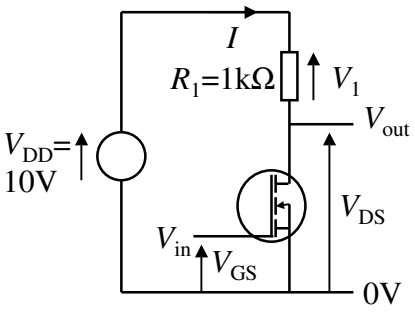
The problem with capacitors is that the voltage across them cannot change instantaneously. Indeed it depends on the rate that charge flows into (or out of) them

When the transistor turns OFF, C charges through R_1. This means the rising edge is slow since it is defined by the large time constant RC

When the transistor turns ON, C discharges through it. The speed of the falling edge is faster since the transistor on resistance is low

n-MOS Logic

- Power consumption is also a problem



Transistor OFF

No problem since no current is flowing through R_1, i.e., V_{out} = 10V

Transistor ON

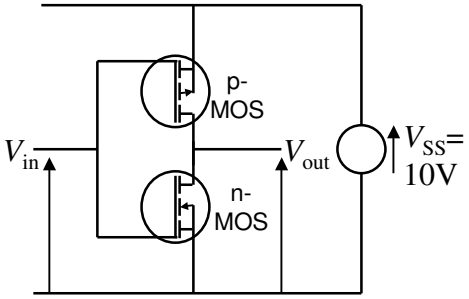
This is a problem since current is flowing through R_1 . For example, if V_{out} = 1V (corresponds with V_{in} = 10V and $I_D = I$ = 9mA), the power dissipated in the resistor is the product of voltage across it and the current through it, i.e.,

$$P_{disp} = I \times V_1 = 9 \times 10^{-3} \times 9 = 81\,\text{mW}$$

CMOS Logic

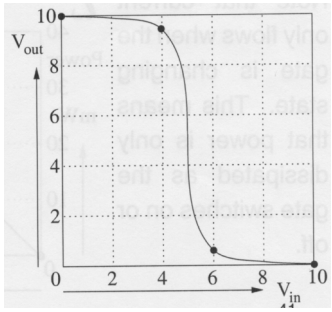
- To overcome these problems, complementary MOS (CMOS) logic was developed
- As the name implies it uses p-channel as well as n-channel MOS transistors
- Essentially, p-MOS transistors are n-MOS transistors but with all the polarities reversed!

CMOS Inverter



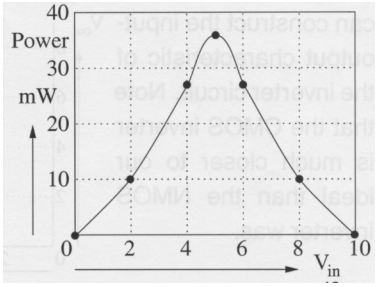
V_{in}	N-MOS	P-MOS	V_{out}
low	off	on	high
high	on	off	low

Using the graphical approach we can show that the switching characteristics are now much better than for the n-MOS inverter



CMOS Inverter

- It can be shown that the transistors only dissipate power while they are switching.



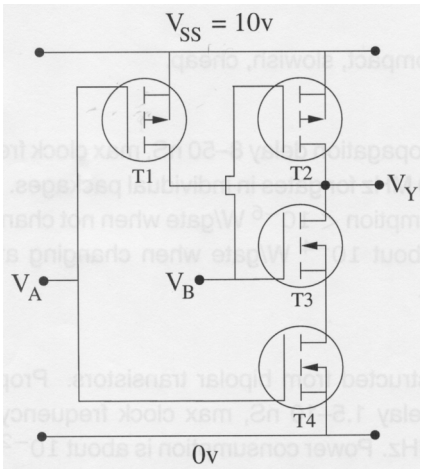
This is when both transistors are on. When one or the other is off, the power dissipation is zero

CMOS is also better at driving capacitive loads since it has active transistors on both rising and falling edges

CMOS Gates

- CMOS can also be used to build NAND and NOR gates
- They have similar electrical properties to the CMOS inverter

CMOS NAND Gate



V_A	V_B	T1	T2	T3	T4	V_Y
low	low	on	on	off	off	high
low	high	on	off	on	off	high
high	low	off	on	off	on	high
high	high	off	off	on	on	low

Logic Families

- **NMOS** – compact, slow, cheap, obsolete
- **CMOS** – Older families slow (4000 series about 60ns), but new ones (74AC) much faster (3ns). 74HC series popular
- **TTL** – Uses bipolar transistors. Known as 74 series. Note that most 74 series devices are now available in CMOS. Older versions slow (LS about 16ns), newer ones faster (AS about 2ns)
- **ECL** – High speed, but high power consumption

Logic Families

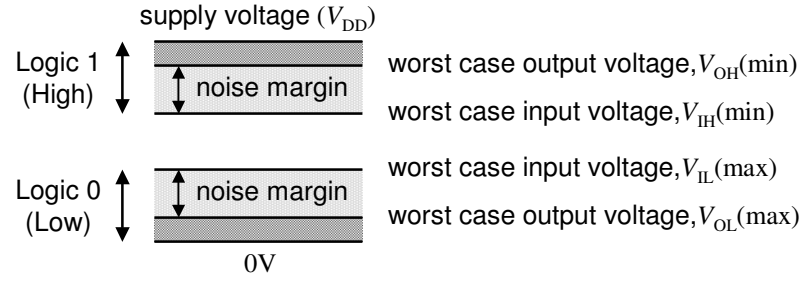
- Best to stick with the particular family which has the best performance, power consumption cost trade-off for the required purpose
- It is possible to mix logic families and sub-families, but care is required regarding the acceptable logic voltage levels and gate current handling capabilities

Meaning of Voltage Levels

- As we have seen, the relationship between the input voltage to a gate and the output voltage depends upon the particular implementation technology
- Essentially, the signals between outputs and inputs are ‘analogue’ and so are susceptible to corruption by additive noise, e.g., due to cross talk from signals in adjacent wires
- What we need is a method for quantifying the tolerance of a particular logic to noise

Noise Margin

- Tolerance to noise is quantified in terms of the noise margin



Logic 0 noise margin = $V_{IL}(\max) - V_{OL}(\max)$

Logic 1 noise margin = $V_{OH}(\min) - V_{IH}(\min)$

Noise Margin

- For the 74 series High Speed CMOS (HCMOS) used in the hardware labs (using the values from the data sheet):

  Logic 0 noise margin = $V_{IL}(\max) - V_{OL}(\max)$

  Logic 0 noise margin = $1.35 - 0.1 = 1.25$ V

  Logic 1 noise margin = $V_{OH}(\min) - V_{IH}(\min)$

  Logic 1 noise margin = $4.4 - 3.15 = 1.25$ V

  See the worst case noise margin = 1.25V, which is much greater than the 0.4 V typical of TTL series devices. Consequently HCMOS devices can tolerate more noise pick-up before performance becomes compromised