Power Optimized 10Gbps Optical Transceivers

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INTRODUCTION

Within the **INTERNET project** we aim at providing **energy-efficient solutions** for optical networks by:

1) assessing the ***power use of physical layers(PHY) of optical transceivers*** by synthesizing corresponding implementations to ASICs,

2) designing burst mode PHY protocols suitable for power gated or optically switched links

RESULTS

Power characterization of 10Gbps PHY designs

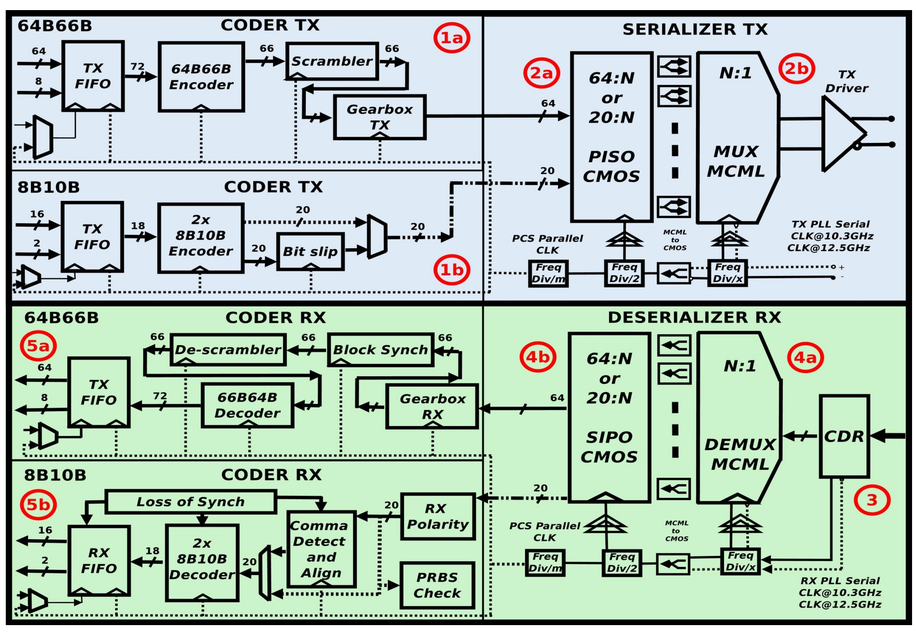


Figure 1: Top-level diagram of the 10Gbps transceiver with 8B10B and 64B66B codecs

The power characterization was carried out for the existing **transceiver architectures** in standard 45nm CMOS process, including **the breakdown** into 8B10B/64B66B coding, serialisation, frame alignment, clock/data recovery functions and, comparison of these to the low-power silicon front-end components.

Power breakdown for 10Gbps transceivers

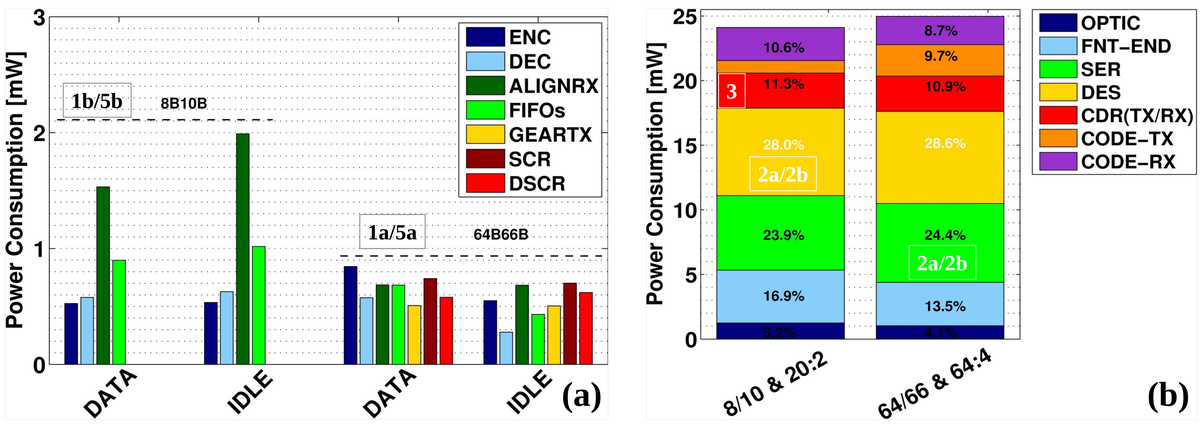


Figure 2: (a) Coding block power; (b) Distribution of power including front-end circuits.

- Power consumption of coders is ***highly workload-dependent*** with 8B10B power being ***inversely-proportional*** to incoming traffic
- High-speed MCML blocks power is ***dominant*** (**~64%**) in the transceiver's profile and is mostly ***optimization-dependent***

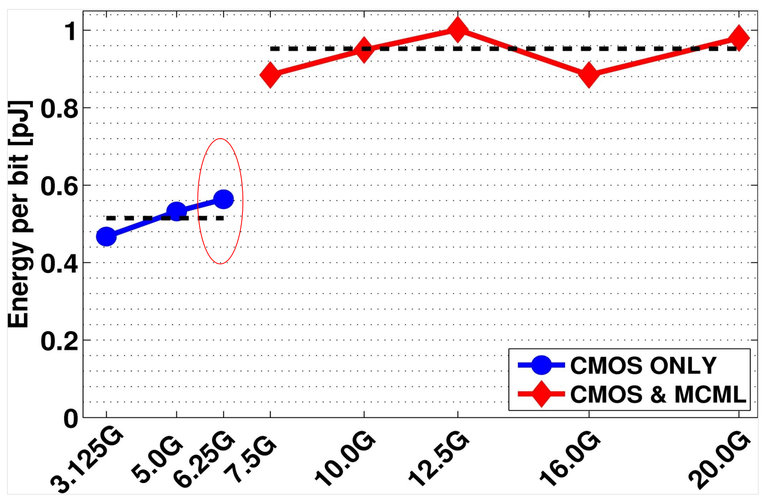
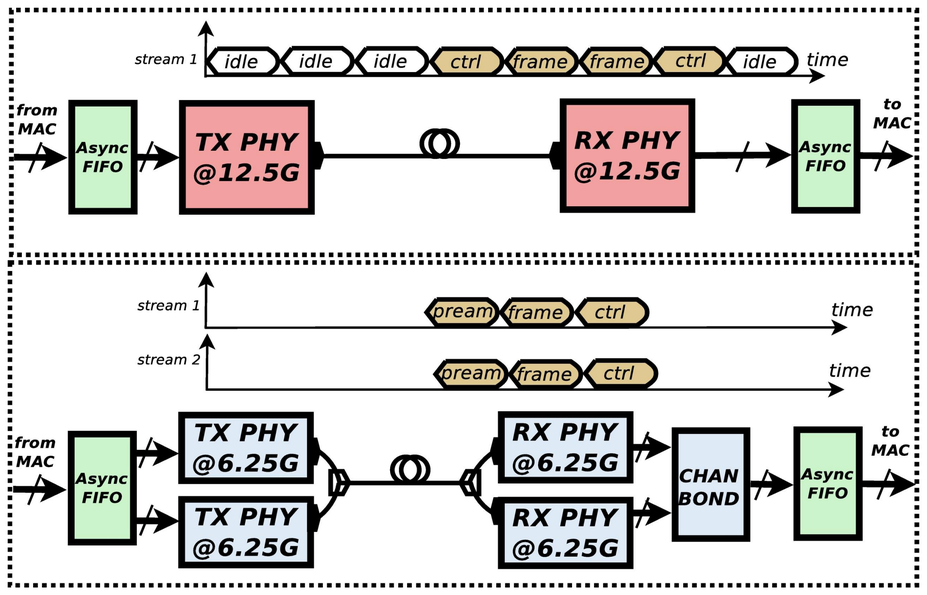


Figure 3: Energy per bit for SERDES circuits

Comparison of **CMOS only** SERDESs efficiency with their **CMOS/MCML variants** shows the **optimal bit rate** of **6.25Gbps**

POWER OPTIMIZED PROTOCOLS

Continuous versus burst mode operation



Hence we proposed 8B10B codec based PHY, optimized for low power burst mode applications. The bit rate per wavelength of 6.25Gbps was chosen to eliminate MCML circuitry from the SERDES and minimize energy per bit.

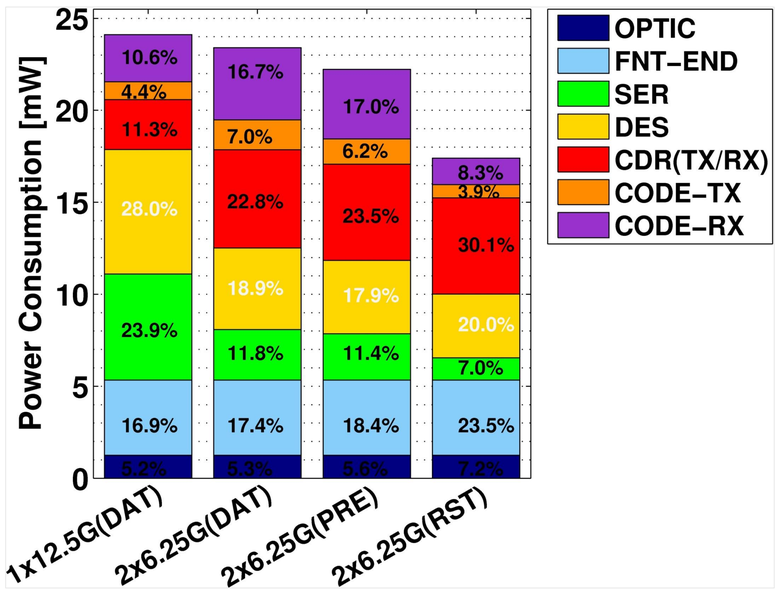


Figure 4: Power characteristics of 6.25 Gbps optically switched transceivers

- Even without power-gating, the burst mode transceiver provides 2% (data), 8% (preamble) and 29% (standby) reduction in power compared to the conventional design.

PERSPECTIVES

The effective energy saving for the representative Ethernet trace with 8.79% link utilization collected within a 24h period constitutes 26.5%

Future work will study:

- Effect of power gating on the system's response time and power profile
- Variations on realistic traffic profiles and their impact on system's stability
- Design and tuning of the front-end driving and equalizing electronics