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A dynamic-logic PLA on low-temperature polysilicon TFT technology

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Motivated by improvements in low-temperature polysilicon thin-film transistor (LTPS-TFT) processes, we designed a TFT-based dynamic-logic programmable logic array (PLA). We report the successful operation of the circuit with high repeatability. We thus demonstrate that the LTPS-TFT technology is mature enough to support aggressive circuit techniques such as dynamic logic.

Introduction: In the domain of flat-panel liquid crystal displays (LCDs), both pixel-switching elements and driving circuits typically employ thin-film transistors, primarily due to their low cost. To ensure correct operation, it is essential that the off-state leakage current of TFT pixel switches be kept as low as possible. This observation dictated investigations aiming at understanding [1] and suppressing [2] the typically high leakage current of polysilicon TFTs. There have also been other improvements in the quality of TFTs, such as better electrical stability and higher carrier mobility values. Thus, opportunities exist to use TFT technologies in large-area electronics applications that are not directly related to LCDs. For example, OLED driver circuits [3], fingerprint sensors [4] and recently an 8-bit processor [5] have been demonstrated. We embarked on an experimental investigation of whether the recently improved leakage current properties of LTPS-TFTs are

suitable for the devices to form dynamic logic circuits. For that purpose, we fabricated a small programmable logic array employing dynamic logic on polysilicon TFT technology. This letter outlines the PLA configuration and presents our findings and conclusions.

PLA Structure: For the purposes of our experiment, we chose a variation of the PLA first presented in standard CMOS technology in [6]. In our version we opted for single-rail asynchronous control [7]. The PLA as such could equally well work synchronously; however, it would be difficult to route a global clock distribution tree in a large-scale design using TFTs, given that LTPS-TFT technologies typically employ a limited number of metal layers. Fig. 1 shows the PLA structure in detail. It consists of AND- and OR-planes, and an interplane buffer. Asynchronous control is realized by two Muller C-elements with a delay line between them. The output of the first C-element (signal Req_internal) plays the same role as the clock signal in the synchronous counterpart as indicated by “Clock” in Fig. 1. When Req_internal=0, points X1 and X4 get charged to logic “high” through the *p*-channel TFTs MP1 and MP3 (“precharge” phase). In the subsequent “evaluate” phase (Req_internal=1), the PLA primary inputs at the gates of *n*-channel TFTs MN2_1-MN2_n determine whether X1 will be discharged to ground, or retain its high voltage. After two inverter delays, the NAND gate in the interplane buffer allows the logic value at X1 to propagate to X3. The final PLA output will depend on whether or not point X4 gets discharged during “evaluate”, that is on the values of all AND-plane results, directed to transistors MN4_1-MN4_m.

The above description is typical of PLA designs, and indeed of dynamic logic in general. Non-standard elements in Fig. 1 include the NAND gate instead of a simple inverter in the interplane buffer, keeper TFT MP2, as well as the use of TFT MN1 between MP1 and the parallel MN2_i TFTs, instead of a ground switch. Detailed justification on these can be found in [6]; with respect to the purposes of this letter, it is evident that if the pull-down *n*-channel TFTs experience high leakage current, then points X1 and X4 may be partially discharged unexpectedly and the circuit may not operate correctly, especially at low frequencies. Our results will confirm that the off-current in LTPS-TFTs is sufficiently low.

Experimental Results: We designed a small PLA together with input latches for the primary inputs and return-to-zero (RTZ) output latches [7] to store the produced outputs. The circuit was fabricated on glass substrate using LTPS-TFT technology. The PLA receives three inputs *A*, *B* and *C*, and implements three logic functions, *S*, *D* and *P*, as follows:

$$S = A\,B\,\overline{C} + A\,\overline{B}\,C + \overline{A}\,B\,C + \overline{A}\;\overline{B}\;\overline{C}$$

$$D = \overline{A}\;\overline{B} + \overline{A}\;\overline{C} + \overline{B}\;\overline{C}$$

$$P = A\,\overline{C} + \overline{B}\,C + \overline{A}\,B$$

We performed measurements with a 5 Volt power supply on 12 individual PLA samples located in different parts of the 300mm×300mm substrate. We fed both external “request” and “acknowledge” signals (Req_in and Ack_out in Fig. 1 respectively) with square waveforms of the same frequency, with an arbitrary phase delay between them. This way, we imitated the assumed

handshaking behaviour, whereby initially the “left-hand side environment” asserts Req_in (first square wave). The circuit output is evaluated; Req_out is asserted and the output latches store the produced value. The “right-hand side environment” uses the output as desired, and then asserts Ack_out (second, delayed, square wave). At this point the PLA output is not needed anymore and the output latches are safely reset to the 0 value. In order to use the PLA again, the “left-hand side environment” needs to drive Req_in to 0, thus causing a new precharge phase, to be followed by the next evaluate operation.

Experiments were conducted with four combinations of input vectors (A,B,C)={(0,0,0),(0,0,1),(0,1,1),(1,1,1)}. Since the Boolean expressions in functions S, D and P are symmetrical, it was not necessary to include other test vectors. We observed that all 12 samples produced the expected outputs correctly. The maximum Req_in operating frequency for our circuit samples spread between 390 and 480 KHz. Fig. 2 shows one of the measured output waveforms of the latch fed by the output of function D, with respect to control lines Req_in and Ack_out, for (A,B,C)=(0,0,0), at 100 KHz. Here, an expected output value of logic 1 was observed approximately 1.3μs after the rising edge of Req_in (the timing depends on the number of inverters in the delay line between the two Muller C-elements in Fig. 1). Given that we used RTZ output latches, output D returns to zero after Ack_out is asserted. After de-asserting both Req_in and Ack_out, the PLA is ready to receive the next set of inputs and produces an output at the next Req_in=1 phase (not shown in Fig. 2).

Conclusion: By fabricating a small PLA on TFTs and experimentally confirming its consistently correct operation, we have demonstrated that dynamic logic can safely be used in modern low-temperature polysilicon TFT technology. We are using such PLA structures in an on-going larger-scale project [8]. It can be predicted that other transistor-level design styles like domino logic, that also depend on sufficiently low leakage current, can also be safely employed. Circuit designers working on modern TFT technologies can therefore use more aggressive and powerful VLSI techniques than in the past.

References

1 LUI, O. K. B., QUINN, M.J., TAM, S.W.-B., BROWN, T.M., MIGLIORATO, P., and OHSHINA, H. : 'Investigation of the Low Field Leakage Current Mechanism in Polysilicon TFTs', IEEE Transactions on Electron Devices, January 1998, Vol. 45, No. 1, pp. 213–217

2 CHANG, K.-M., YANG, W.-C., and TSAI, C.-P. : 'Performance and Reliability of Low-Temperature Polysilicon TFT With a Novel Stack Gate Dielectric and Stack Optimisation Using PECVD Nitrous Oxide Plasma', IEEE Transactions on Electron Devices, January 2004, Vol. 51, No. 1, pp. 63–67

3 TAM, S.W.-B., BOERO, M., and MIGLIORATO, P. : 'Poly-Si Driving Circuits for Organic EL Displays', Proceedings of SPIE, Conference 4295A, Electronic Imaging 2001, pp. 125

4 MIYASAKA, M., HARA, H., TAKAO, H., TAM, S.W.-B., PAYNE, R., RAJALINGHAM, P., INOUE, S., SHIMODA, T. : 'Flexible Microelectronics: New Application for Thin-Film Transistors in Fingerprint Sensors', Journal of the Society for Information Displays, March 2005, Vol. 13, No. 3, pp. 187-191

5 KARAKI, N., NANMOTO, T., EBIHARA, H., UTSUNOMIYA, S., INOUE, S., SHIMODA, T. : 'A Flexible 8-bit Asynchronous Microprocessor Based on Low-Temperature Poly-Silicon Technology', Digest of Technical Papers of the 52nd IEEE International Solid-State Circuit Conference (ISSCC) 2005, pp. 272-273

6 WANG, J.-S., CHANG, C.-R., and YEH, C. : 'Analysis and Design of High-Speed and Low-Power CMOS PLAs', IEEE Journal of Solid-State Circuits, August 2001, Vol. 36, No. 8, pp. 1250-1262

7 SPARSØ, J., and FURBER, S. : 'Principles of Asynchronous Circuit Design – A Systems Perspective', Kluwer Academic Publishers, 2001

8 OIKONOMAKOS, P., FOURNIER, J., and MOORE, S. : 'Implementing Cryptography on TFT Technology for Secure Display Applications', Springer LNCS Proceedings of the 7th IFIP International Conference on Smart Card Research and Advanced Applications (CARDIS) 2006, pp. 32-47

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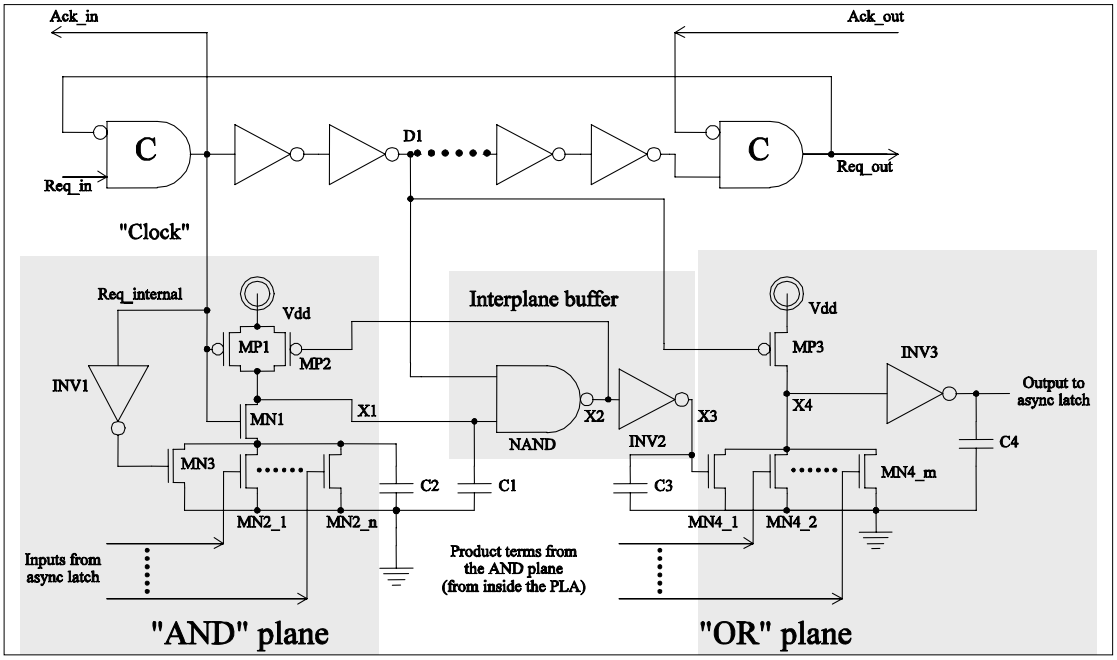
Figure captions:

Fig. 1 PLA configuration

Fig. 2 Measured PLA output (function *D*, (*A*,*B*,*C*)=(0,0,0), 100 KHz)

Figure 1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Ack_out
C
C
D1
Req_in
Req_out
"Clock"
Req_internal
Vdd
MP1
MP2
INV1
MN1
X1
Interplane buffer
NAND
X2
X3
INV2
Vdd
MP3
INV3
Output to
async latch
X4
C4
MN3
C2
C1
C3
MN4_m
MN2_1
MN2_n
MN4_1
MN4_2
Inputs from
async latch
Product terms from
the AND plane
(from inside the PLA)
"AND" plane
"OR" plane

Figure 2